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Regular Paper

Electrical Properties Based on Dielectric Layer Thickness for the Optimal Design of $BaTiO_3$-Based X8R MLCCs

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Abstract: This study investigates the effect of dielectric layer thickness on the electrical and reliability characteristics of $BaTiO_3$-based X8R multilayer ceramic capacitors (MLCCs) for automotive applications. MLCCs with 30 dielectric layers and thicknesses ranging from 5 to 30 μm were fabricated, and key parameters—including capacitance, equivalent series resistance (ESR), insulation resistance (IR), breakdown voltage (BDV), DC-bias characteristics, temperature coefficient of capacitance (TCC), and ripple current-induced heating—were evaluated. The dielectric constant (~2,000) and sintering shrinkage (~–25%) were nearly independent of thickness, confirming stable microstructure formation. ESR increased with thickness, while normalized BDV (V/μm) decreased due to defect accumulation. IR improved with increasing thickness but dropped sharply above 125°C. Dielectrics thinner than 10 μm exhibited significant capacitance degradation under DC-bias and temperature variation, reflecting strong internal field effects. Ripple-induced heating correlated directly with ESR. These results indicate that, although thinner layers enhance capacitance density, reducing the thickness below 10 μm compromises bias stability and thermal reliability. A minimum dielectric thickness of 10 μm is therefore recommended to achieve an optimal balance between electrical performance and durability in high-reliability X8R MLCCs.

Keywords: BaTiO, Dielectric, BME MLCC, X8R, TCC, High reliability

1. INTRODUCTION

MLCCs have become indispensable components in modern electronic systems due to their high volumetric efficiency, low equivalent series resistance (ESR), and excellent reliability. In recent years, the demand for MLCCs with enhanced thermal and electrical stability has significantly increased, particularly in applications such as automotive electronics, high-power conversion systems, and AI data center power supplies, where devices must operate reliably under high-temperature and high-voltage conditions. To ensure stable performance in such harsh environments, the X8R dielectric class has been established as a key standard, requiring that capacitance variation remain within ±15% over the temperature range of –55°C to +150°C. Achieving this performance necessitates precise control of both dielectric composition and microstructural uniformity [1-5]. Among various dielectric materials, $BaTiO_3$ is the most widely used base dielectric in MLCCs because of its high dielectric constant and excellent compatibility with Ni internal electrodes. However, $BaTiO_3$-based dielectrics suffer from severe reliability degradation under the reducing atmospheres required for Ni electrode processing. During sintering, partial reduction of Ti^{4+} to Ti^{3+} generates oxygen vacancies, which deteriorate insulation resistance (IR), lower the breakdown voltage (BDV), and accelerate long-term degradation. Therefore, improving the reduction resistance and insulation properties of $BaTiO_3$-based dielectrics has become a central challenge in the development

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of next-generation X8R MLCCs [5-10]. To address these issues, rare-earth oxide doping (e.g., Dy_2O_3, Y_2O_3, Ho_2O_3) has been widely utilized. Rare-earth ions partially substitute for Ba^{2+} or Ti^{4+} sites within the perovskite lattice, suppressing oxygen vacancy formation and compensating charge imbalance through the creation of donor-like defect pairs. Such doping stabilizes the crystal lattice and suppresses electron hopping conduction, thereby enhancing insulation resistance and breakdown voltage under reducing conditions. In particular, Y^{3+} and Yb^{3+} ions can form stable solid solutions in the $BaTiO_3$ lattice, improving grain boundary resistance and maintaining high IR even at elevated temperatures [11-16]. In this study, a Yb_2O_3–Y_2O_3 co-doped $BaTiO_3$-based X8R dielectric composition was employed to simultaneously achieve high reduction resistance and reliability. The co-doping strategy provides a synergistic effect: Y^{3+} acts as a charge compensator, while Yb^{3+} enhances grain boundary resistivity, ensuring excellent insulation performance even at temperatures above 150°C. This composition is well suited for MLCCs operating in high-voltage and high-temperature environments—such as automotive and AI server applications—and offers the advantage of effectively controlling the defect chemistry within the dielectric [17-20]. While numerous studies have investigated the effects of dopant type, firing atmosphere, and grain size on dielectric reliability, relatively few have systematically examined how dielectric layer thickness influences electrical performance under identical material and process conditions. In our previous work, we analyzed the relationship between the number of dielectric layers and electrical characteristics such as breakdown voltage and insulation behavior. However, a quantitative understanding of dielectric thickness, which directly determines internal electric field distribution, polarization behavior, and mechanical constraint between layers, remains insufficient [2.3,5,19,20]. Therefore, in this study, dielectric thicknesses of 5, 10, 20, and 30 μm were used as design variables under identical compositional and processing conditions to evaluate their influence on capacitance, dielectric loss (tan δ), ESR, insulation resistance (IR), breakdown voltage (BDV), RC, DC-bias characteristics, temperature coefficient of capacitance (TCC), and ripple-current-induced heating. By isolating dielectric thickness as the sole variable, the relationships among electric field distribution, defect behavior, and degradation mechanisms in MLCCs could be systematically analyzed. The primary objective of this study is to establish fundamental guidelines for dielectric design that simultaneously achieve high capacitance and high reliability. Through quantitative evaluation of the electrical property variations with dielectric thickness, this work aims to provide design criteria for stable operation in high-temperature and high-voltage environments, such as automotive control modules and AI data-center power units. Ultimately, it was confirmed that Yb_2O_3–Y_2O_3 co-doped $BaTiO_3$-based X8R MLCCs require a minimum dielectric thickness of approximately 10 μm to achieve the optimal balance between capacitance performance and long-term reliability.

2. EXPERIMENTAL

2.1 Fabrication of MLCC Samples

In this study, MLCCs were fabricated using a $BaTiO_3$-MgO-Mn_3O_4-Yb_2O_3-Y_2O_3-V_2O_5-$(BaCa)SiO_3$ dielectric composition optimized for X8R characteristics. The MLCCs were manufactured in 2012 size (2.0 × 1.2 × 0.8 mm) with Ni internal electrodes and Cu/Ni/Sn external electrodes. The number of dielectric layers was fixed at 30, and the dielectric layer thicknesses were set at 5, 10, 20, and 30 μm. The dielectric powders were dispersed with polyvinyl butyral (PVB, Sekisui BM-SZ), an ethanol/toluene mixed solvent, and dioctyl phthalate (DOP, DC Chemical) using a Nano-set mill to prepare a homogeneous slurry. The slurry was cast into green sheets of 5, 10, 20, or 30 μm thickness on PET release films using a slot-die coater. Ni internal electrodes were screen-printed on the green sheets, and 30 layers were laminated to form multilayer bars. The laminated bars were cold isostatically pressed (CIP) and then cut into individual green chips. Binder burnout was performed at 240°C for 72 h. Sintering was carried out at 1,150°C for 2 h under a controlled reducing atmosphere ($PO_2 = 10^{-10}$–10^{-12} MPa, H_2–N_2–H_2O gas mixture), followed by reoxidation at 900°C for 60 min under a mildly oxidative atmosphere ($PO_2 = 10^{-7}$ MPa). After polishing, Cu external electrodes were applied and heat-treated at 800°C, and the MLCCs were finally finished with Ni-Sn plating.

2.2 Characterization of Dielectric Properties

Capacitance and dissipation factor (tan δ) were measured at 1 kHz and 1 Vrms using an LCR meter (Keysight E4980A). C–V characteristics were evaluated by combining the LCR meter with a DC power supply (Keysight E3643A). Insulation resistance (IR) measurements were performed at 25°C, 85°C, 125°C and 150°C using a DC power supply, a digital electrometer, and a high-temperature shielded chamber. Breakdown voltage per unit thickness (BDV) was determined using a dielectric withstand tester (HIOKI 3174) by ramping the DC voltage at 0.5 V/s until the leakage current reached 1 μA. The temperature coefficient of capacitance (TCC) was measured over the range of –25°C to 150°C at 1 kHz using an LCR meter (HP 4284A) in a temperature-controlled chamber. Ripple current-induced heating was assessed by applying AC ripple currents while monitoring the surface temperature rise (ΔT) using infrared thermography.

3. RESULTS AND DISCUSSION

Figure 1 shows the variation of dielectric shrinkage and dielectric constant as a function of dielectric layer thickness in $BaTiO_3$-MgO-Mn_3O_4-Yb_2O_3-Y_2O_3-V_2O_5-(BaCa)SiO_3 MLCCs. The dielectric shrinkage remained relatively constant at approximately –25% across the entire thickness range, with a slight increase observed as the layer thickness decreased. For instance, the shrinkage was –24.22% for a 30 μm thick dielectric layer, while it increased to –26.44% for a 5 μm layer,

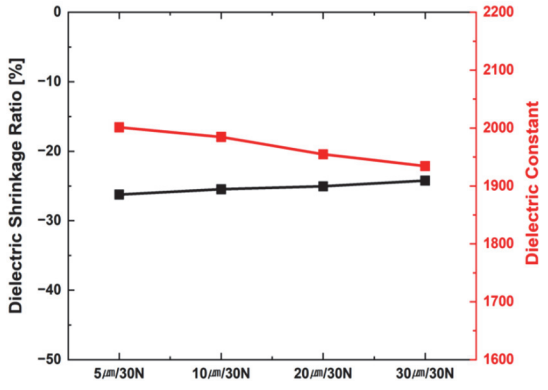

Fig. 1. Dielectric shrinkage and dielectric constant as a function of dielectric layer thickness.

representing an approximate 2% rise. This increase in shrinkage is likely related to the constraint imposed by the internal Ni electrodes during sintering and the residual stress arising from the mismatch in thermal expansion coefficients between the electrodes and the dielectric. Regarding the dielectric constant, a slight increase was observed with decreasing dielectric thickness. The dielectric constant increased from 1,934 at 30 μm to 2,041 at 5 μm, an increment of about 100. This phenomenon can be attributed to enhanced polarization of dielectric domains in the thinner layers due to sintering-induced shrinkage stress and thermal expansion mismatch with the internal electrodes. In other words, as the dielectric layers become thinner, the relative internal stress is higher, favorably promoting domain deformation and thereby increasing the dielectric constant.

Figure 2 shows the relationships between capacitance–ESR and tan δ–ESR for $BaTiO_3$-based multilayer ceramic capacitors (MLCCs) with varying dielectric layer thicknesses, measured at 1 kHz and Vrms = 0.1 V. The results indicate that the capacitance (C) decreases with increasing dielectric thickness, consistent with the parallel-plate capacitor model:

$$C = \frac{\varepsilon_r \varepsilon_0 A}{t}$$

where ε_r is the relative permittivity, A is the electrode area, and t is the dielectric thickness. Under constant permittivity and electrode area, an increase in dielectric thickness results in a corresponding inverse reduction in capacitance.

As the capacitance decreases, the equivalent series resistance (ESR) increases. ESR is generally expressed as:

$$ESR = \frac{\tan\delta}{2\pi f C}$$

Although the dielectric loss (tan δ) showed a slight decrease with increasing layer thickness, the observed change in ESR was primarily governed by the reduction in capacitance rather than tan δ. In other words, the main cause of the ESR increase observed in the Capacitance–ESR relationship is the decrease in capacitance.

A similar trend is observed in the tan δ–ESR curve. While dielectric loss slightly decreases with increasing thickness, ESR increases due to the concurrent reduction in capacitance. This emphasizes the importance of maintaining low ESR in

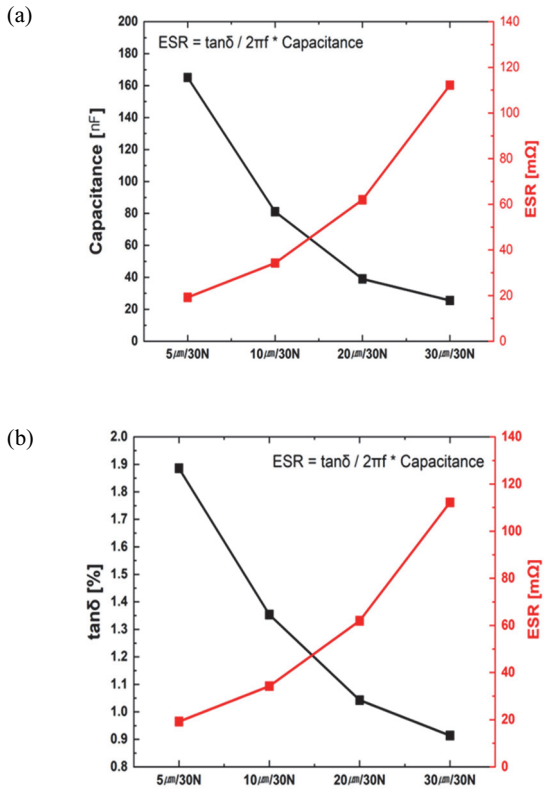

Fig. 2. Capacitance, ESR, and dielectric loss as a function of dielectric layer thickness. (a) Capacitance – ESR and (b) tan δ – ESR.

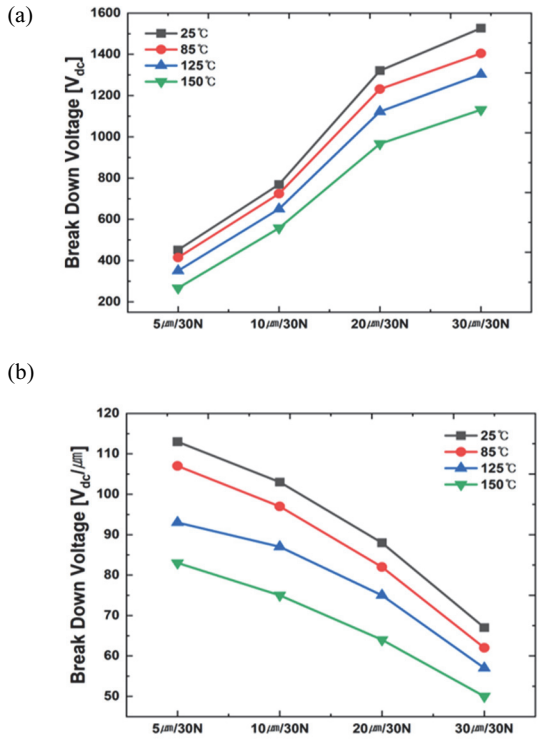

Fig. 3. Breakdown voltage (BDV) and normalized BDV per unit dielectric thickness as a function of dielectric thickness and measurement temperature. (a) Breakdown voltage (BDV) and (b) normalized BDV per unit dielectric thickness.

MLCC design, particularly to minimize self-heating under ripple current operation.

Figure 3 presents the variation of breakdown voltage (BDV) and normalized BDV per unit dielectric thickness as a function of dielectric thickness and measurement temperature. The BDV increases proportionally with the dielectric thickness, which can be attributed to the extended potential path that allows the applied electric field to be more evenly distributed, thereby enhancing the overall dielectric strength. For example, at 25°C, the sample with a 5 μm dielectric layer exhibits a BDV of approximately 400 Vdc, whereas the 30 μm sample shows an increased BDV of about 1,500 Vdc. In contrast, when normalized by dielectric thickness, the BDV per unit thickness [Vdc/μm] decreases inversely with increasing dielectric thickness. This inverse relationship arises from the accumulation of volume-related defects, pores, and grain boundary inhomogeneities that become more probable in thicker dielectrics, leading to localized electric field concentration. Consequently, while the total BDV increases with dielectric thickness, the dielectric strength per unit thickness decreases due to defect accumulation effects. In addition, a common trend of BDV degradation with increasing temperature was observed for all dielectric thicknesses. The maximum BDV was measured at 25°C, and a gradual decrease was observed as the temperature rose to 85°C, 125°C, and 150°C. This degradation is attributed to the thermally activated conduction paths and the increase in leakage current caused by thermal excitation of charge carriers. At elevated temperatures, the mobility of oxygen vacancies within the $BaTiO_3$-based dielectric increases, leading to charge accumulation and local electric field enhancement under applied bias, which accelerates the dielectric breakdown process. Specifically, the BDV at 150°C decreases by approximately 30–40% compared to that at 25°C, and the normalized BDV [Vdc/μm] exhibits a similar declining trend. This behavior indicates that the breakdown voltage depends on the dielectric thickness (d) and temperature (T) according to the following relationships:

$$\text{BDV} \propto d^n \quad (\text{n} < 1), \quad E_{BDV}(T) = E_o \exp\left(-\frac{E_a}{kT}\right)$$

Here, n (n < 1) reflects the cumulative effect of defect generation with increasing thickness, while (E_a) represents the thermal activation energy. Therefore, although the total BDV increases with dielectric thickness, the dielectric strength per unit thickness decreases due to defect accumulation, and higher temperatures accelerate thermally activated conduction and defect migration, leading to a further reduction in BDV.

Figure 4 presents the variation in insulation resistance (IR) and RC product (R·C) as functions of dielectric thickness and measurement temperature. As shown in Fig. 4(a), IR increases significantly with increasing dielectric thickness due to the reduced electric field intensity per unit thickness, which suppresses charge-carrier migration and leakage current pathways. In contrast, IR decreases with increasing temperature following a thermally activated conduction mechanism, exhibiting a similar trend to the breakdown voltage (BDV) behavior shown in Fig. 3.

To quantitatively analyze the temperature dependence, the IR data were fitted using the Arrhenius relation:

$$\text{R}(T) = R_o \exp\left(\frac{E_a}{K_B T}\right)$$

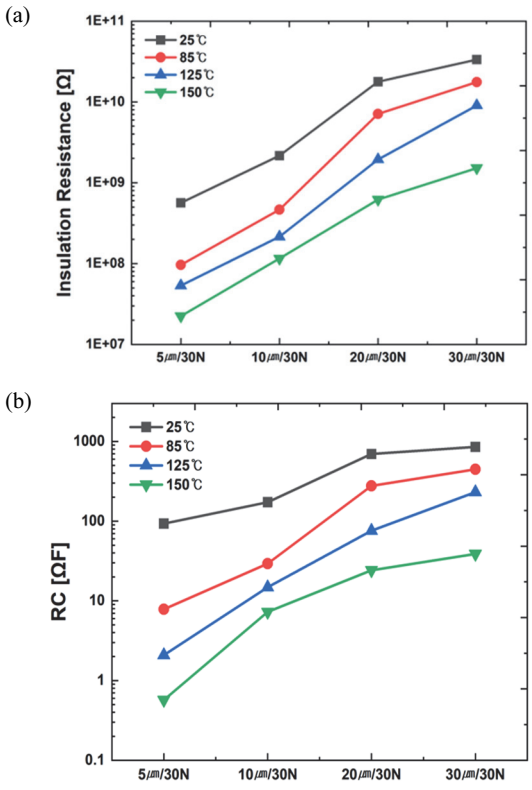

Fig. 4. Insulation resistance and the R·C as a function of dielectric thickness and measurement temperature. (a) Insulation resistance and (b) R · C value.

The extracted activation energies (Ea) were 0.82 eV for the 30 µm sample, 0.77 eV for 20 µm, 0.70 eV for 10 µm, and 0.65 eV for 5 µm. This monotonic decrease in Ea with decreasing thickness indicates that thinner dielectric layers contain shallower defect levels, facilitating thermal excitation and migration of charge carriers and thereby activating leakage conduction paths.

Meanwhile, Fig. 4(b) shows the RC product, defined as the product of resistance (R) and capacitance (C), which reflects both dielectric polarization and leakage behavior. The RC value increases with increasing dielectric thickness, indicating enhanced charge-storage capability and insulation stability. However, it decreases sharply with increasing temperature due to thermally activated leakage current. At 150°C, samples with dielectric thicknesses below 10 µm exhibit RC values below 10 Ω·F, indicating severe degradation in insulation stability. These findings demonstrate that thermally activated leakage in thin dielectrics significantly deteriorates insulation performance. Therefore, for X8R-type dielectrics, maintaining a dielectric thickness of at least 10 µm is crucial to ensure reliable insulation stability under high-temperature operating conditions.

Figure 5 shows both (a) the capacitance degradation (ΔC–Vdc) under applied DC voltage for different dielectric thicknesses and (b) the capacitance change normalized by dielectric thickness (ΔC–Vdc/µm). The DC-bias (C–V) characteristic of MLCCs represents the change in capacitance when a DC voltage is applied across the device. Under DC bias, the dielectric constant of the ceramic material decreases nonlinearly due to polarization saturation within the ferroelectric domains, as the applied electric field aligns dipoles in the dielectric, reducing overall permittivity and thus capacitance. In Fig. 5(a), thinner dielectric layers exhibit more pronounced capacitance reduction: at 50 Vdc, a 30 µm dielectric layer shows only about –6 % reduction, whereas a 5 µm layer exhibits approximately –60 %, nearly a tenfold difference, indicating that thinner layers are more sensitive to DC bias and that the effective capacitance in circuit operation

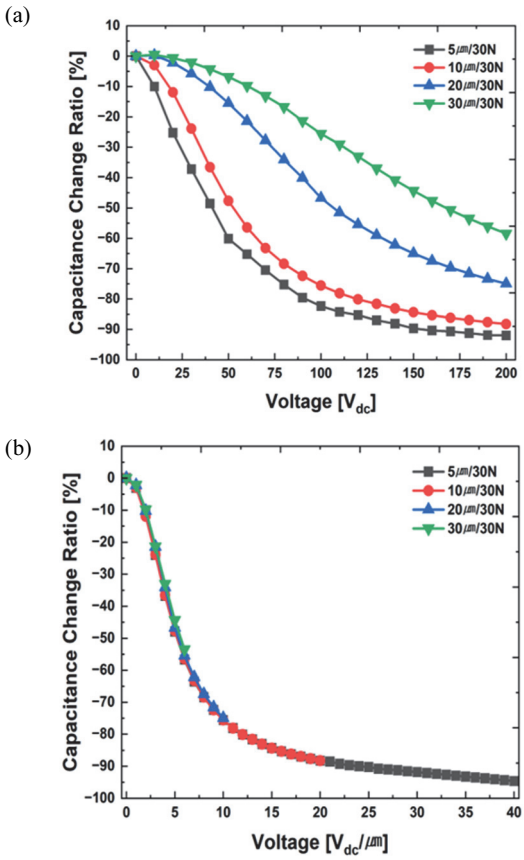

Fig. 5. DC-bias and normalized C–V as a function of dielectric thickness and measurement temperature. (a) DC-bias and (b) normali zed C–V.

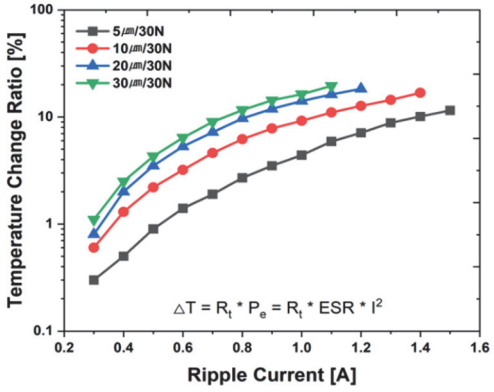

Fig. 6. Self-heating temperature change ratio as a function of dielectric thickness and ripple current.

can deviate significantly from the nominal value. In Fig. 5(b), when the capacitance variation is normalized by dielectric thickness, the results converge across all thicknesses, demonstrating that DC-bias behavior is governed by the intrinsic permittivity response of the dielectric material rather than by layer thickness. The consistent normalized response reflects dielectric polarization per unit field, associated with domain dynamics described by the P–E hysteresis behavior of $BaTiO_3$-based ceramics. Consequently, C–V performance improves with increasing dielectric thickness, while the intrinsic material response per unit thickness remains constant, confirming that high C–V performance in MLCC design can be achieved by employing thicker dielectric layers to effectively mitigate DC-bias-induced degradation without altering the intrinsic material characteristics.

Figure 6 illustrates the self-heating characteristics of MLCCs as a function of dielectric layer thickness and applied ripple current. For MLCCs with a fixed number of dielectric layers (N = 30) and electrode area, an increase in dielectric thickness reduces the capacitance. The reduction in Capacitance leads to an increase in equivalent series resistance (ESR), which is the direct cause of enhanced heat generation under ripple current. The resulting temperature rise can be expressed by Joule heating as $\Delta T = Rt \cdot Pe = Rt \cdot I^2R$. Consequently, MLCCs with thinner dielectric layers exhibit lower ESR and reduced self-heating, whereas thicker dielectrics show higher ESR and greater temperature rise. Therefore, the observed increase in self-heating with dielectric thickness is attributed not to the thickness itself, but to the capacitance-dependent increase in ESR. In MLCC design, dielectric thickness, ESR, and thermal dissipation must be considered collectively to ensure reliable operation under ripple current conditions.

Figure 7 illustrates the actual thermal dissipation path model of an MLCC under ripple-current excitation. The current flows through a thermal path composed of internal electrodes, dielectric, and external electrodes, where losses originating from ESR components are converted into heat. As the dielectric layer becomes thinner, the electric field intensity and current density within each layer increase, resulting in greater power dissipation across the ESR region. Because metallic Ni electrodes possess higher thermal conductivity than the ceramic dielectric, the generated heat is preferentially transferred and concentrated along the electrode interfaces. Consequently, as the ripple current increases, the temperature rise exhibits a nonlinear dependence on current magnitude. IR thermography measurements further confirm localized

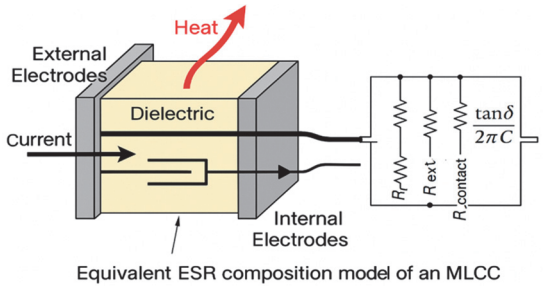

Fig. 7. The actual thermal dissipation path model of an MLCC under ripple-current excitation.

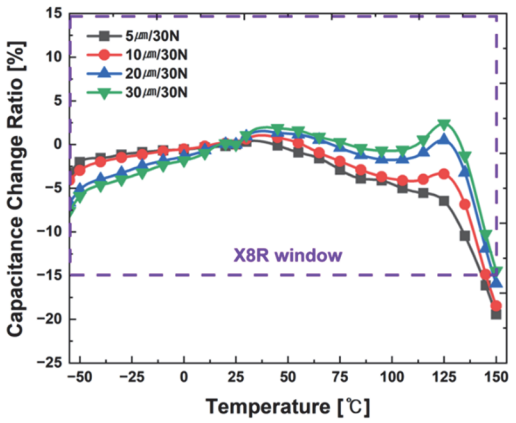

Fig. 8. TCC as a function of dielectric thickness and temperature.

temperature concentration near the electrode regions [21]. Such ripple-induced self-heating behavior critically contri–butes to reliability degradation and insulation-resistance deterioration in MLCCs.

Figure 8 shows the temperature coefficient of capacitance (TCC) characteristics of MLCCs as a function of dielectric layer thickness, illustrating capacitance variation over a temperature range from –55°C to +150°C. As the dielectric layer becomes thinner, the capacitance variation at low temperatures (–55°C) increases positively, while at high temperatures (+150°C), the variation becomes more negative, indicating that dielectric thickness strongly influences both the capacitance and TCC characteristics of MLCCs. The pronounced TCC change in thin dielectric layers at high temperatures can be attributed to the temperature-dependent permittivity behavior of the ceramic dielectric. In ferroelectric ceramics such as $BaTiO_3$-based MLCCs, the relative permittivity (ε_r) is highly sensitive to temperature due to domain dynamics and phase transitions. Thinner dielectric layers experience stronger internal electric fields under the same applied voltage, which enhances dipole alignment and amplifies the temperature-induced variation of permittivity. As the temperature rises, thermal fluctuations further destabilize the dipole alignment, causing a larger decrease in ε_r and, consequently, a greater reduction in capacitance. In contrast, thicker dielectric layers distribute the internal electric field more uniformly, reducing the sensitivity of permittivity to temperature changes and resulting in smaller TCC variation.

These results indicate that the high-temperature TCC degradation observed in thin dielectric MLCCs is closely related to the intrinsic temperature dependence of the ceramic dielectric and its nonlinear response under strong internal electric fields.

4. CONCLUSION

In this study, MLCCs were fabricated using a $BaTiO_3$-MgO-Mn_3O_4-Yb_2O_3-Y_2O_3-V_2O_5-$(BaCa)SiO_3$ dielectric composition optimized for X8R characteristics. The influence of dielectric layer thickness on the electrical performance and reliability of $BaTiO_3$-based X8R MLCCs was systematically investigated. Samples with 30 dielectric layers and individual layer thicknesses of 5, 10, 20, and 30 μm were prepared under identical compositional and processing conditions, and key parameters—including capacitance, ESR, insulation resistance, breakdown voltage, DC-bias characteristics, temperature coefficient of capacitance (TCC), and ripple-current-induced self-heating—were evaluated.

The results indicate that capacitance decreases inversely with increasing dielectric thickness, whereas ESR increases, resulting in higher self-heating under ripple current for thicker layers. Breakdown voltage increased with total dielectric thickness; however, when normalized per unit thickness, it tended to decrease due to defect accumulation. Insulation resistance improved with increasing thickness but exhibited a sharp decline above 125°C. DC-bias testing showed that thinner dielectric layers suffered more pronounced capacitance degradation due to stronger internal electric fields, whereas thicker layers demonstrated more stable C–V characteristics. TCC analysis revealed that thinner dielectrics experienced significant high-temperature degradation, primarily due to the temperature-dependent permittivity of $BaTiO_3$ and enhanced dipole reorientation under strong internal fields.

These findings underscore that dielectric layer thickness is a critical parameter in balancing performance and reliability in MLCC design. Thinner layers offer higher capacitance density but are more vulnerable to DC-bias effects, thermal degradation, and insulation instability. In contrast, thicker layers enhance reliability at the cost of volumetric efficiency. Based on these results, a minimum dielectric thickness of 10 μm is recommended to achieve stable performance and long-term reliability under high-voltage and high-temperature operating conditions.

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