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Analytical Drain-Induced-Barrier-Lowering Model of Elliptic Gate-All-Around FET with Ferroelectric

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Abstract: Drain Induced Barrier Lowering (DIBL) was analyzed when the channel of Gate-All-Around (GAA) FET, which is the most promising in the miniaturizing transistor structure, has an elliptic cross-section. The oxide film structure used a stacked Metal-Ferroelectric-Metal-Insulator-Semiconductor (MFMIS) structure using SiO_2 and ferroelectric. An analytical DIBL model was presented to analyze the DIBL in elliptic GAA FET with ferroelectric. Its validity was proven by comparing the results of other papers. As a result, the Drain Induced Barrier Rising (DIBR) effect, that is, the negative DIBL effect, appeared depending on the ferroelectric thickness t_{fe}, and the ratio of the remanent polarization P_r and coercive field E_c in the ferroelectric, P_r/E_c. The DIBL varied linearly with $t_{fe}E_c/P_r$, and the slope depended on the rate of change for the drain voltage of the ferroelectric charge Q, dQ/dV_{ds}. The $t_{fe}E_c/P_r$ value satisfying DIBL=0 mV/V decreased as eccentricity increased. The ferroelectric thickness t_{fe} will have to be decreased because the subthreshold swing increases if the P_r/E_c is increased to reduce the $t_{fe}E_c/P_r$ value. The threshold voltage increased at this time, but the effect was minimal.

Keywords: Elliptic, Gate-All-Around, DIBL, Eccentricity, Ferroelectric

1. INTRODUCTION

The reduction in the actual size of the FET is an important factor in reducing production costs due to increased integration in wafers, and improving transistor performance. However, according to the scaling theory of the transistor, the threshold voltage cannot be scaled down as much as the transistor size is reduced due to the supply voltage limit and higher power consumption [1-3]. Additionally, an increase in static power consumption is a major problem due to the subthreshold swing, which is limited to 60 mV/dec by Boltzmann Tyranny. To solve this problem, efforts are being made to use ferroelectric in the gate oxide film. When ferroelectric is stacked with inner gate metal and used as a gate oxide film, a negative capacitance effect occurs due to hysteresis characteristics. It means the subthreshold swing can be reduced to less than 60 mV/dec [4-6]. Additionally, the threshold voltage is reduced due to the voltage amplification phenomenon of the inner gate voltage [7-9]. HfZrO is used as the ferroelectric because it is excellently compatible with the CMOS process. Because the threshold voltage changes due to the ferroelectric, it will eventually affect drain-induced-barrier-lowering (DIBL). In other words, when ferroelectric is used as the gate oxide film, not only DIBL reduction phenomenon but also negative DIBL, known as drain induced barrier rising (DIBR) phenomenon, occurs depending on ferroelectric thickness [10-12]. Changing from positive DIBL to negative DIBL due to ferroelectric ultimately means that there exists a condition where DIBL=0 mV/V. In this paper, we seek to obtain the condition of DIBL=0 mV/V in an elliptic Gate-All-Around (GAA) FET with ferroelectric.

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GAA FET has a structure that surrounds the channel with a gate terminal. It can control the flow of carriers in the channel more efficiently than FinFET [13-15]. Leading global semiconductor companies such as Samsung Electronics and TSMC are also competing to produce microstructure FETs using GAA FETs. In particular, the ultimate structure that can solve the corner effect that occurs in square structures will be a cylindrical structure. In addition, to improve the current level, it is manufactured in the form of a Multi-Bridge Channel FET [16,17]. However, it is impossible to manufacture a cylindrical GAA FET with a completely circular cross-section of the channel.

Therefore, research is being conducted on the GAA FETs with an elliptical cross-sectional area that inevitably occurs during the process [18,19]. Research on elliptic GAA FETs was actively conducted about 10 years ago, but little research has been conducted recently [20,21]. Most of the research analyzed the characteristics for the aspect ratio (AR), which is the ratio of the major axis and minor axis of an ellipse. The problem here was to fix the major axis or minor axis and change the AR by adjusting the rest [22,23]. In this case, the characteristics of the transistor will naturally change because the channel cross-sectional area changes. Therefore, the change in DIBL was calculated for an ellipse with the same cross-sectional area in this paper. Chiang recently analyzed the short channel subthreshold current according to the interface trap charge using the potential model of an elliptic GAA FET [24].

Since it was found that the subthreshold swing can be reduced to less than 60 mV/dec by using ferroelectric, research on other short channel effects such as DIBL is necessary for the GAA FET with ferroelectric [25,26]. If no ferroelectric is used, negative DIBL does not occur and DIBL=0 mV/V could not be obtained even in the case of the elliptic GAA FET [27]. Therefore, the use of ferroelectric is essential to obtain DIBL=0 mV/V. Since the DIBL ultimately represents the change in the threshold voltage, the analysis of the threshold voltage must be performed first. In the case of the elliptic GAA FET with ferroelectric, the threshold voltage has a constant value depending on P_r/E_c, the ratio of the remanent polarization P_r of the ferroelectric and the coercive electric field E_c [28]. Therefore, DIBL will also have a constant value depending on P_r/E_c. The DIBL of the elliptic GAA FET with ferroelectric will change depending on the ferroelectric thickness and P_r/E_c, and in the case of HfZrO, it mostly exists within the range of 5 pF/cm$< P_r/E_c <$30 pF/cm, so DIBL was considered in this range and ferroelectric thickness was calculated for 0~20 nm. The channel structure used a junctionless. This structure is known to solve the process problems that occur in junction-based FETs because the source/drain and channel are manufactured with the same doping type and similar doping concentration. At this time, the gate structure will use the metal-ferroelectric-metal-insulator-semiconductor (MFMIS) structure. This structure can more effectively solve the field nonuniformity problem occurring in the metal-ferroelectric-insulator-semiconductor (MFIS) structure, and Cheng et al. compared these two structures [29].

2. STRUCTURE AND DIBL MODEL OF AN ELLIPTIC JUNCTIONLESS GAA FET WITH FERROELECTRIC

2.1 Structure of an elliptic junctionless GAA FET with ferroelectic

Figure 1 is a schematic diagram of the elliptic GAA FET with ferroelectric used in this paper. As shown in Fig. 1, the MFMIS structure is used, and the gate applied voltage is V_{gs2} applied to the outer metal. The induced voltage of the inner metal is V_{gs1}. Ferroelectric used parameters for HfZrO, and as mentioned in the already published paper [28], DIBL was obtained for the general values of permanent polarization P_r and coercive electric field E_c. In particular, DIBL is constant for P_r/E_c, the ratio of P_r and E_c, and was compared in the range of 5 pF/cm $< P_r/E_c <$ 30 pF/cm. The insulator was SiO_2. The eccentricity, which changes depending on the aspect ratio ($AR=b/a$), which is the ratio of the length a of the major axis and the length b of the minor axis of the elliptic FET, is determined by the channel cross-sectional area πR^2 of the standard circular GAA FET and the channel cross-sectional area πab of the elliptic GAA FET. The DIBL was obtained when its areas were the same, that is, when the eccentricity changed with $R^2 = ab$. The channel material was silicon, the channel doping was N-type, and the concentrations were 10^{18}/cm^3 or 10^{19}/cm^3 as junctionless. The device parameters used in this paper are listed in Table 1.

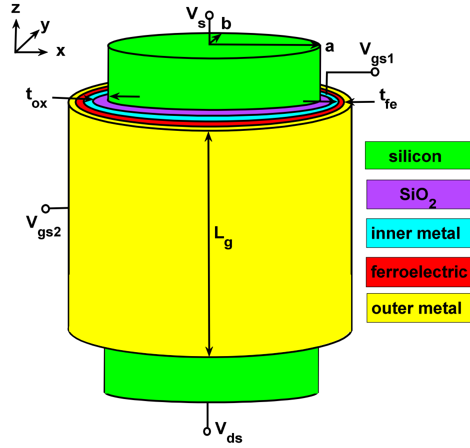

Fig. 1. Overview of an elliptic junctionless GAA FET with ferroelectric.

Table 1. Device parameters for this analytical SS model.

Device parameter	Symbol	Value
Channel length	L_g	15~100 nm
Channel radius	R	5 nm
Oxide thickness	t_{ox}	1~2 nm
Ferroelectric thickness	t_{fe}	0~20 nm
Doping concentration	N_d	10^{18}, 10^{19}/cm^3
Ratio of P_r and E_c	P_r/E_c	5~30 pF/cm
Eccentricity	e	0~0.99

2.2 DIBL models of an elliptic junctionless GAA FET with ferroelectric

The relationship between the major and minor axis to have the same area as a circle with radius R is given in Eq. (1) for the eccentricity e of an ellipse.

$$e=\sqrt{1-\left(\frac{b}{a}\right)^2},\ b=R\left(1-e^2\right)^{\frac{1}{4}},\ a=\frac{R^2}{b} \tag{1}$$

To obtain DIBL in the MFMIS structure, the change in threshold voltage relative to the drain voltage must first be obtained. In the junctionless structure, the threshold voltage was defined as the gate voltage when the minimum voltage in the channel was V_{bi}-$2V_t$. This definition was valid in an already published paper [30]. In other words,

$$\begin{aligned}&\phi_{C\min}(z=z_{\min})=2\sqrt{AB}+\varphi_{CL}=V_{bi}-2V_t\\&\varphi_{CL}=V_{gs1}-V_{fb}+\frac{qN_d\lambda^2}{\varepsilon_{si}}\end{aligned} \tag{2}$$

where V_{bi} is the junction potential of the source/drain as the reference voltage, and V_t is kT/q defined by the Boltzmann constant k and the absolute temperature T. V_{gs1} is the inner gate voltage, V_{fb} is the flat-band voltage, ε_{si} is the dielectric constant of silicon, and λ is the scaling length given in Chiang's paper [24]. In Eq. (2), the variables A and B are derived using Chiang's potential model and are given in Eq. (3).

$$\begin{aligned}&A=\frac{\left(V_{bi}-\varphi_{CL}\right)\left(e^{\frac{L_g}{\lambda}}-1\right)-V_{ds}}{2\sinh\left(\frac{L_g}{\lambda}\right)}=a_1V_{gs1}+a_2\\&B=\frac{V_{ds}-\left(V_{bi}-\varphi_{CL}\right)\left(e^{-\frac{L_g}{\lambda}}-1\right)}{2\sinh\left(\frac{L_g}{\lambda}\right)}=a_3V_{gs1}+a_4\end{aligned} \tag{3}$$

As can be seen from the previous paper [27], by substituting Eq. (3) into Eq. (2) and solving for V_{gs1}, the threshold voltage for the corresponding drain voltage V_{ds} can be obtained using Eq. (4).

$$\begin{aligned}&V_{th1}=\frac{-B_1+\sqrt{B_1^2-4A_1C_1}}{2A_1}\\&A_1=\left(4a_1a_3-1\right)\\&B_1=\left[4\left(a_1a_4+a_2a_3\right)+2\left(V_{fb}-\frac{qN_D\lambda^2}{\varepsilon_{si}}+V_{bi}-2V_t\right)\right]\\&C_1=4a_2a_4-\left(V_{fb}-\frac{qN_D\lambda^2}{\varepsilon_{si}}+V_{bi}-2V_t\right)^2\end{aligned} \tag{4}$$

This is the threshold voltage of the inner gate, and it is necessary to obtain the threshold voltage V_{th2} for the actual applied voltage V_{gs2}. For this purpose, the relationship with ferroelectric charge Q and ferroelectric voltage V_{fe}, that is, Eq. (5), must be used.

$$\begin{aligned}&V_{fe}=2\alpha t_{fe}Q+4\beta t_{fe}Q^3+6\gamma t_{fe}Q^5\\&\alpha=-\frac{3\sqrt{3}}{4}\frac{E_c}{P_r}\,(m/F),\ \beta=\frac{3\sqrt{3}}{8}\frac{E_c}{P_r^3}\,(m^5/F/C^2),\ \gamma=0\end{aligned} \tag{5}$$

There is a relationship between V_{th1} of the inner gate and V_{th2} of the outer gate as shown in the following Eq. (6).

$$V_{th2} = V_{th1} + V_{fe} \tag{6}$$

Using this relationship, the DIBL of an elliptic GAA FET with ferroelectric can be obtained using Eq. (7).

$$DIBL = -\frac{dV_{th2}}{dV_{ds}} = -\left(\frac{dV_{th1}}{dV_{ds}} + \frac{dV_{fe}}{dV_{ds}}\right) \tag{7}$$

The dV_{th1}/dV_{ds} in Eq. (7) can be obtained from an already published paper [27]. The change in ferroelectric voltage V_{fe} for the drain voltage V_{ds} can be obtained as the following Eq. (8) using Eq. (5).

$$\frac{dV_{fe}}{dV_{ds}} = 2t_{fe}\left(\alpha + 6\beta Q^2\right)\frac{dQ}{dV_{ds}} \tag{8}$$

Using the ferroelectric charge Q obtained from an already published paper [25], dQ/dV_{ds} in Eq. (8) can be obtained as in the following Eq. (9).

$$\frac{dQ}{dV_{ds}} = \left(\frac{C_{ox}}{2\pi L_g\sqrt{(a^2+b^2)/2}}\right)\left(\frac{1}{2\sinh(L_g/\lambda)}\right)\left[\lambda(1-e^{-\frac{L_g}{\lambda}}) + \lambda(1-e^{\frac{L_g}{\lambda}})\right] \times \int_0^{\pi}\sqrt{a^2\cos^2\theta + b^2\sin^2\theta}\left\{1-\left(\frac{a^2\cos^2\theta}{2\lambda_a^2} + \frac{b^2\sin^2\theta}{2\lambda_b^2}\right)\right\}d\theta \tag{9}$$

Here, C_{ox} is oxide capacitance, and the integral is obtained using MATLAB's *integral* command. The λ_a and λ_b are indicated in [24]. When calculating dV_{th1}/dV_{ds} and dQ/dV_{ds}, the elliptical cross-sectional shape of the channel is reflected in a, b, and scaling length λ.

In the case of the GAA FET with MFMIS structure, it has already been announced that the threshold voltage appears constant for a given P_r/E_c. Therefore, to first consider the change in threshold voltage to drain voltage, the change in threshold voltage for P_r/E_c is calculated using Eq. (2) with aspect ratio AR and drain voltage V_{ds} as parameters, when the ferroelectric thickness is t_{fe}=10 nm as shown in Fig. 2. As shown in Fig. 2, the threshold voltage decreased as P_r/E_c increased. However, the reduction rate changes depending on AR and V_{ds} and the distribution of threshold voltage is divided into DIBL and DIBR area. That is, in the region where P_r/E_c is small, it is in the DIBR area, but when P_r/E_c increases, it

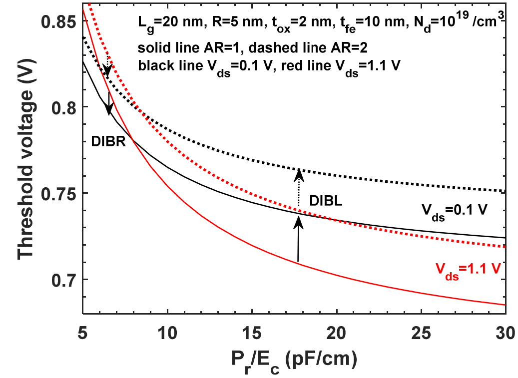

Fig. 2. Threshold voltages for P_r/E_c with AR and V_{ds} as parameters under the given conditions in figure.

changes to the DIBL area. In other words, it can be observed that the threshold voltage increases or decreases as the drain voltage increases depending on P_r/E_c. As P_r/E_c increases, DIBL increases. Comparing the cases of AR=1 and AR=2, it can be observed that DIBL decreases in the case of AR=2. Additionally, the threshold voltage increases as AR increases.

To examine in detail the change in threshold voltage depending on eccentricity and the presence or absence of ferroelectric, Fig. 3 shows the change in threshold voltage with the presence or absence of ferroelectric and drain voltage as parameters. As shown in Fig. 2, since the DIBR effect does not appear in the case of P_r/E_c = 10 pF/cm, the DIBR effect was calculated for the case where the ferroelectric thickness was 20 nm. As shown in Fig. 3, in the case of t_{fe}=20 nm, it can be observed that the DIBR effect occurs due to ferroelectricity. It can be seen that DIBL decreases in the absence of ferroelectric and DIBR decreases in the presence of ferroelectric as eccentricity increases. The changes in DIBL (DIBR) for eccentricity begin to appear above e=0.8, which means that AR is about 2. In other words, it can be seen that the change of the threshold voltage of the elliptic GAA FET does not appear according to eccentricity when AR < 2. In this way, it can be seen that the change in threshold voltage for eccentricity is ultimately caused by the change in minimum central potential [27]. In other words, it can be seen that as the eccentricity increases, the minimum central potential decreases and the threshold voltage that satisfies Eq. (2) increases. Minimum central potential changes not only depending on eccentricity but also on drain voltage, so the threshold voltage changes not only on drain voltage but also

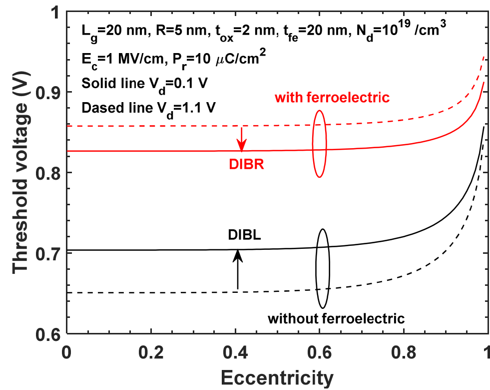

Fig. 3. Threshold voltages for the eccentricity with the presence or absence of ferroelectric and drain voltage V_{ds} as parameters.

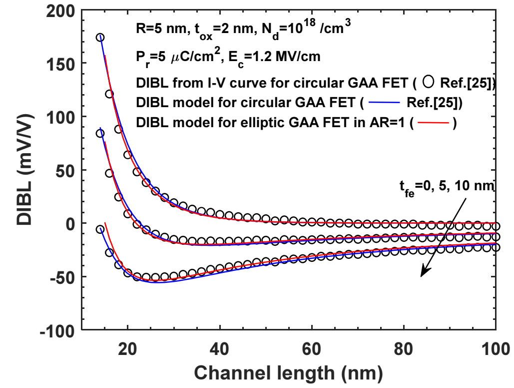

Fig. 4. Comparisons with the results for the previous paper [28] and this DIBL model.

on ferroelectric thickness and eccentricity as can be seen in Figs. 2 and 3, so DIBL will also change accordingly. This paper will closely observe the changes in DIBL for changes in the ferroelectric thickness and eccentricity.

3. VERIFICATION AND ANALYSIS OF THIS DIBL MODEL OF AN ELLIPTIC JUNCTIONLESS GAA FET WITH FERROELECTRIC

To prove the validity of the DIBLs obtained using Eqs. (4), (7), (8), and (9), the results were compared with the results of a previously published paper in Fig. 4. As shown in Fig. 4, the previously announced circular GAA FET model and the elliptic GAA FET presented in this paper were compared for the case of $a = b$ i.e. $AR = 1$, and the results match well. Here, the results matched well even if the ferroelectric thickness changed. Therefore, in the case of elliptic GAA FET with ferroelectric, the change in the DIBLs according to eccentricity will be analyzed using the DIBL model presented in this paper.

In Fig. 5, the change in the DIBL according to the eccentricity is shown with P_r/E_c and ferroelectric thickness as parameters. The DIBL can be observed to decrease as the eccentricity increases in the area of 10 pF/cm < P_r/E_c <30 pF/cm. Also, it can be seen that DIBL at t_{fe}=0 nm, that is, in the case without ferroelectric, is always larger than in the case with ferroelectric. Therefore, DIBL can be reduced using ferroelectric, and a negative DIBL or DIBR effect was shown depending on the conditions. As P_r/E_c decreased, DIBL

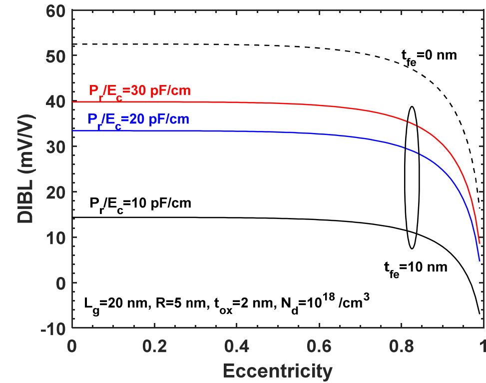

Fig. 5. The DIBLs for eccentricity with ferroelectric thickness and P_r/E_c as parameters.

decreased, and this was accompanied by a decrease in subthreshold swing [26]. As shown in Fig. 5, as P_r/E_c becomes smaller, negative DIBL appears. In Fig. 5, it can be observed that the DIBL becomes saturated as P_r/E_c increases. As P_r/E_c increases, it ultimately means that the hysteresis characteristics of the ferroelectric weaken, so it will ultimately converge to the DIBL of t_{fe}=0 nm.

The change in DIBL is shown for P_r/E_c using t_{fe} and AR as parameters in Fig. 6. As shown in Fig. 6, it can be observed that it eventually approaches the DIBL in t_{fe}=0 nm as P_r/E_c increases. In addition, the DIBL was decreased when AR=2 compared to AR=1, and a negative DIBL or DIBR effect was observed when t_{fe}=10 nm at P_r/E_c <6 pF/cm. The change in DIBL became more severe as t_{fe} increased and P_r/E_c decreased. Comparing the curves of AR=1 and AR=2 in Fig. 6, it can be seen that as P_r/E_c decreases, the effect on DIBL gradually

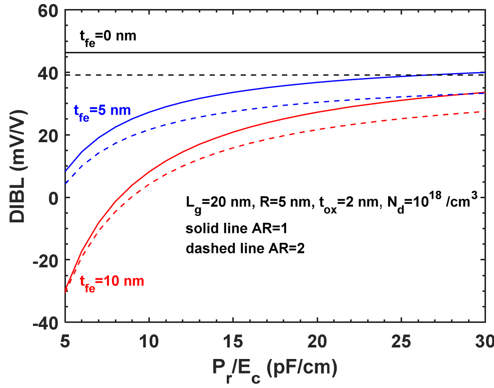

Fig. 6. The DIBLs for P_r/E_c with the ferroelectric thickness and eccentricity as parameters.

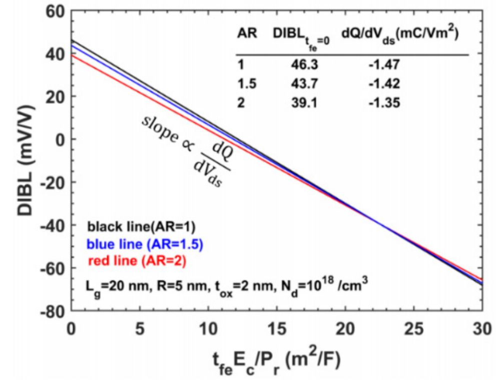

Fig. 7. The DIBLs for $t_{fe}E_c/P_r$ with AR as a parameter.

decreases even if the cross-sectional area changes from a circle to an ellipse. It can be seen that the factors affecting the DIBL are ultimately t_{fe} and P_r/E_c, in the case of elliptic GAA FET with ferroelectric.

In an ideal device, the value of DIBL=0 mV/V should be maintained. Comparing the two terms in the parentheses of Eq. (8), since $6\beta Q^2$ is much smaller than α, the factor affecting DIBL will ultimately be the $t_{fe}E_c/P_r$ value depending on α in Eq. (5). That is, Eq. (7) can be expressed as Eq. (10).

$$DIBL = \frac{3\sqrt{3}}{2}\left(\frac{dQ}{dV_{ds}}\right)\left(\frac{t_{fe}E_c}{P_r}\right) + DIBL_{t_{fe}=0} \tag{10}$$

In Fig. 7, the change in DIBL according to the $t_{fe}E_c/P_r$ value is shown with AR as a parameter. As shown in Fig. 7, the DIBL value at t_{fe}=0 nm is the value of $-dV_{thl}/dV_{ds}$ without ferroelectric. Additionally, the dQ/dV_{ds} value in Eq. (8) can be obtained from the slope of each straight line. As shown in Fig. 7, when AR = 1, dQ/dV_{ds} = -1.47 mC/Vm^2, and when AR = 2, dQ/dV_{ds} = -1.35 mC/Vm^2. It can be seen that the smaller the absolute value of dQ/dV_{ds}, the smaller the change in DIBL for $t_{fe}E_c/P_r$. As shown in Fig. 7, DIBL decreases as AR increases when $t_{fe}E_c/P_r$ < 22.5 m^2/F, but DIBL increases when $t_{fe}E_c/P_r$ > 22.5 m^2/F as AR increases. Therefore, if E_c/P_r is too small, DIBL increases when AR increases. It can be seen that DIBL always decreases as eccentricity increases at ferroelectric thickness t_{fe}=0 nm [27].

As shown in Fig. 7, the $t_{fe}E_c/P_r$ values satisfying DIBL=0 mV/V decrease when AR increases. To examine this in more detail, the relationship between $t_{fe}E_c/P_r$ and eccentricity that

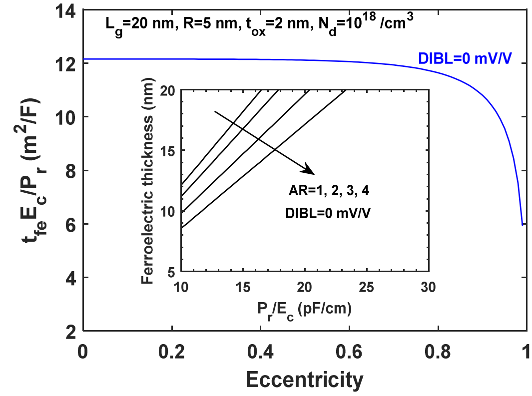

Fig. 8. The $t_{fe}E_c/P_r$ value for the eccentricity satisfying DIBL=0 mV/V.

satisfies DIBL=0 mV/V is shown in Fig. 8. The inset of Fig. 8 shows the relationship between the ferroelectric thickness t_{fe} and E_c/P_r that satisfies DIBL=0 mV/V under given conditions. In the inset of Fig. 8, it can be seen that the slope becomes smaller as AR increases. The slope represents the $t_{fe}E_c/P_r$ value that satisfies DIBL=0 mV/V at the corresponding AR value. It can be observed that the slope becomes smaller as AR increases. The slope for the corresponding eccentricity, that is, $t_{fe}E_c/P_r$ values is indicated by a blue line. It can be observed that the $t_{fe}E_c/P_r$ rapidly decreases when the eccentricity is above 0.8. A decrease in the $t_{fe}E_c/P_r$ ultimately means a decrease in t_{fe} or an increase in P_r/E_c. Since an increase in P_r/E_c ultimately leads to an increase in subthreshold swing, it would be desirable to reduce t_{fe} to set DIBL=0 mV/V. However, a decrease in the ferroelectric thickness will decrease the

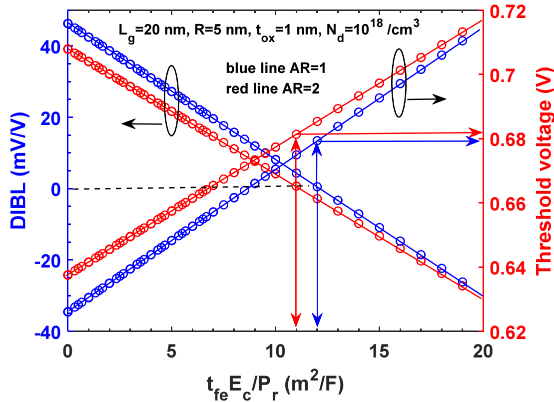

Fig. 9. The relationship of $t_{fe}E_c/P_r$ and threshold voltage to satisfy DIBL=0 mV/V with AR as a parameter.

effectiveness of utilizing the ferroelectric while causing a decrease in remanent polarization and retention and an increase in subthreshold swing. Therefore, the ferroelectric thickness and the ratio of P_r/E_c should be determined by considering the trade-off between subthreshold swing and DIBL.

To consider the change in the threshold voltage, the relationship between DIBL and the threshold voltage is shown for $t_{fe}E_c/P_r$ in Fig. 9 using AR as a parameter when the cross-sectional area of the channel changes from a circle to an ellipse while maintaining DIBL = 0 mV/V. As shown in Fig. 9, when AR increases, that is, when eccentricity increases, the $t_{fe}E_c/P_r$ value to satisfy the DIBL=0 mV/V becomes smaller as explained in Fig. 8. However, as shown in Fig. 9, the threshold voltage value increases for $t_{fe}E_c/P_r$ value corresponding to the DIBL=0 mV/V value at AR=2. In other words, as eccentricity increases, the threshold voltage also increases. As described above, when AR increases, t_{fe} must be decreased rather than increasing P_r/E_c to satisfy the DIBL=0 mV/V value. This is because the subthreshold swing increases as P_r/E_c increases.

4. CONCLUSIONS

In the case of the elliptic junctionless GAA FET with ferroelectric, the relationship among factors affecting DIBL was compared and investigated. For this purpose, an analytical DIBL model was presented, and it was observed that it was in good agreement with the results derived from current-voltage characteristics in other papers. Because it is difficult to manufacture a circular structure during the process, research on GAA FETs with an elliptic cross section is considered very important. In addition, factors affecting DIBL that inevitably occur in microdevices were analyzed. Due to the presence of ferroelectric, the DIBR effect was appearing depending on t_{fe} and P_r/E_c. As a result, when the ferroelectric thickness and the ratio of P_r/E_c were constant, DIBL also showed a constant value. The change in DIBL for $t_{fe}E_c/P_r$ was linear, and the slope changed depending on the degree of change in the drain voltage of the ferroelectric charge. In other words, the degree of change in DIBL for $t_{fe}E_c/P_r$ decreased as the absolute value of dQ/dV_{ds} became smaller. As eccentricity increased, the $t_{fe}E_c/P_r$ value satisfying DIBL=0 mV/V decreased. At this time, if the P_r/E_c value is increased, the subthreshold swing increases, so the t_{fe} value must be decreased. Additionally, it was found that as eccentricity increases, the threshold voltage increases at the $t_{fe}E_c/P_r$ value that satisfies DIBL=0 mV/V. However, the effect increased by about 1% when increasing from AR=1 to AR=2, showing a very slight effect. Because it is difficult to manufacture a perfectly circular GAA FET during the process, analysis of the elliptic GAA FET is inevitable. In particular, the MFMIS structure is a structure that can reduce the short channel effects in transistors that are becoming miniaturized, so research on this should continue. In fact, as the eccentricity increases, the cross-sectional area of the channel will become rectangular rather than circular. If the eccentricity increases excessively like this, the advantages of the circular cross-sectional GAA FET will disappear and parasitic effects may occur. Therefore, it is necessary to find the condition for DIBL=0 mV/V by controlling the ferroelectric thickness and P_r/E_c rather than adjusting the eccentricity. We are currently studying the effects of P_r and E_c, two factors that determine the material properties of ferroelectrics, on negative differential resistance by analyzing the change in drain current for drain voltage in MFMIS GAA FETs. This study will serve as a cornerstone for developing devices and circuits using ferroelectrics in the future.

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