

Terminal Configuration and Growth Mechanism of III-V on Si-Based Tandem Solar Cell: A Review

Alamgeer¹, Muhammad Quddamah Khokhar², Muhammad Aleem Zahid²,
Hasnain Yousuf¹, Seungyong Han¹, Yifan Hu², Youngkuk Kim³,
Suresh Kumar Dhungel³ , and Junsin Yi^{1,2,3} 

¹ Interdisciplinary Program in Photovoltaic System Engineering, Sungkyunkwan University, Suwon 16419, Korea

² Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon 16419, Korea

³ College of Information and Communication Engineering, Sungkyunkwan University, Suwon 16419, Korea

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Abstract: Tandem or multijunction solar cells (MJSCs) can convert sunlight into electricity with higher efficiency (η) than single junction solar cells (SJSCs) by dividing the solar irradiance over sub-cells having distinct bandgaps. The efficiencies of various common SJSC materials are close to the edge of their theoretical efficiency and hence there is a tremendous growing interest in utilizing the tandem/multijunction technique. Recently, III-V materials integration on a silicon substrate has been broadly investigated in the development of III-V on Si tandem solar cells. Numerous growth techniques such as heteroepitaxial growth, wafer bonding, and mechanical stacking are crucial for better understanding of high-quality III-V epitaxial layers on Si. As the choice of growth method and substrate selection can significantly impact the quality and performance of the resulting tandem cell and the terminal configuration exhibit a vital role in the overall proficiency. Parallel and Series-connected configurations have been studied, each with its advantage and disadvantages depending on the application and cell configuration. The optimization of both growth mechanisms and terminal configurations is necessary to further improve efficiency and lessen the cost of III-V on Si tandem solar cells. In this review article, we present an overview of the growth mechanisms and terminal configurations with the areas of research that are crucial for the commercialization of III-V on Si tandem solar cells.

Keywords: Si-Substrate, Growth techniques, III-V/Si solar cells, Terminals configuration, Tandem solar cells

1. INTRODUCTION

Solar power generation has turned considerably more attractive than conventional energy production concerning the economy and environmental protection due to gradually reduced production costs and increased power conversion

✉ Junsin Yi; junsin@skku.edu

Suresh Kumar Dhungel; suresh@skku.edu

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efficiency of photovoltaic (PV) modules [1]. The capacity for minimizing the overall cost is confined until the efficiency of solar cells (SCs) is further enhanced, emerging in a considerably high module and installed system expense [2]. Due to the significant improvements in the crystalline silicon (c-Si) industry, Si-based SCs over the past few years occupies a major part of PV technology possessing a market dominance of more than 90% due to which the production cost of Si-based SCs has therefore significantly decreased. The maximum power conversion efficiency (PCE) achieved for single junction (SJ) Si-SCs is 26.7% [3], whereas the theoretical

efficiency boundary of Si-solar cell is 29.4% [4], indicating the full performance utilization edge of SJ Si-solar cell which will be completely employed in near future. For this purpose, one of the significant approaches to further improve the PCE of SCs is to introduce the multi-junction (MJ) technique, which allows the different bandgaps solar cell materials to be stacked on one another which can further harness the excellent absorption spectrum of the sun [5,6]. Furthermore, tandem architecture enhances cell performance by decreasing thermalization and below-bandgap losses. It, therefore, consists of various lattice parameters and bandgaps accessibility [7]. However, III-V compounds in MJSCs acquired the record high photoconversion efficiency (PCE) of 38.8% in one sun and [8] up to 46% [9] in concentrated sunlight. However, among various types of solar cells, III-V on Si tandem SCs have gained significant consideration owing to its ability to combine the high proficient III-V materials with inexpensive and scalable Si substrates. The growth of III-V materials on Si substrates possesses several challenges i.e. lattice mismatch, thermal expansion mismatch, as well as interfacial defects. Understanding the growth mechanism and terminal configuration of III-V on Si tandem SCs is crucial for optimizing their performances and realizing their full potential.

Despite the remarkable proficiency of III-V/Si tandem SCs, the low market ratio of III-V in PV power production is primarily due to its expensive manufacturing costs [10]. However, amongst the entire modules which are essential to construct III-V MJSCs, its vital aspect is the expense of the initial substrate, such as the substrate price of Ge or GaAs. Moreover, Si as a substrate has various benefits over GaAs or Ge substrates such as a greater diameter and lower cost correspondingly. Furthermore, Si substrates also offer distinctive benefits in terms of mechanical durability and thermal conductivity. An effort can be employed to integrate Si substrates with III-V compound semiconductors to lower the price of energy leveling. Therefore, the substrates of Si are preferred over Ge as a base of conventional dual-junction (2J) InGaP/GaAs SCs, specifically in the aspect of both current as well as the matching bandgap of Si (0.67 eV) and (1.12 eV) Ge respectively. However, theoretical findings indicated that InGaP/GaAs//Si as 3 J SCs can however the quickest path to acquire maximum efficiency for III-V on Si tandem SCs exhibiting theoretical efficiency surpassing 40% [11]. Research outputs have indicated that there is an almost 70%

[12] drop in the overall cost of tandem SCs when a shift from Ge to Si substrates occurs. Additionally, when employing Si as a passive initial model, the III-V tandem cells have the benefit of more organized methods (i.e. spalling and epitaxial lift-off) decreasing the cost deprived of lowering cell performance [13]. In the early 1980s, numerous organizations and enterprises began inquiring about the assimilation of III-V materials on Si substrates based on its significance in PVs. Though, the production of imperfections throughout the compound development and issues with consistency and reliability limits the effectiveness of III-V on Si tandem SCs compared to numerous other tandem approaches. In recent years, tandem SCs based on III-V/Si are yet again attaining vital consideration because of the growing heteroepitaxy growth, wafer bonding, and mechanical stacking which, therefore, effectively addressed the issues. Furthermore, the incorporation of III-V on Si substrates can grasp considerable capacity due to the declining expense of Si and the significant opportunity for enhancement in the working, particularly in the performance of III-V SCs [5,13].

In this review article, a detailed survey of the III-V on Si tandem SCs is reported. The article is organized as follows. In section 2, three distinct configurations of tandem cell terminals (T) such as 2T, 3T, and 4T in III-V/Si tandem SCs together with three separate mechanisms of growth for III-V compounds on Si substrates are discussed, respectively. In section 3, the research importance for the commercialization of III-V/Si tandem SCs is discussed in brief accordingly. In section 4, the conclusion of this review article is presented with the prospective and potential difficulties faced for the fabrication of high-efficiency III-V/Si tandem SCs.

2. CONFIGURATION OF TERMINALS

Figure 1 illustrates the three main terminal configurations utilized for tandem solar cells based Si in combination with III-V Materials, along with relevant real-world applications [12-14]. The only known combinations are wafer bonding or 2T tandems. The complexity of cell interconnections may be significantly reduced in photovoltaic modules by using 2T tandem topologies as a direct substitute for SJSCs. On the other hand, 2T tandem configurations have very clear disadvantages. Current matching conditions rigorously

confine the materials that can be used for the top cell, and it is likely that resistance as well as optical losses, therefore, lower the efficiency of the cell. As a result, 4T tandem structures are often manufactured by mechanical stacking, rendering them resistant to sub-cell current matching. However, there are two issues with 4T tandem configurations: they have a high resistance that is difficult to reduce, and the top cell's back contact results in optical losses that involve transmission and reflection. The 4T tandem topologies can also stop heteroepitaxial development and make module-level integration of cells more complex, which might further increase production costs. The shortcomings of the two prior tandem designs are also recommended to be addressed by the 3T tandem arrangement. However, the 3T tandem design is consistent with the other two most common compound growth methods since the intermediary connections for lateral current transfer are not required in this case [12].

The 2T cell is associated with a junction tunnel. The 3T sub-cells are linked through a TCA, and the 4T cell has a glass interlayer that electrically segregates the sub-cells. The top cell of III-V is further attached to the glass and therefore

stacked with an interdigitated back contact (IBC) Si bottom cell in the 3T and 4T terminal configurations.

For discovering material and design vulnerability, cell-level degradation analysis is essential. Comparing III-V/Si tandem SCs to other hybrid tandem approaches, the extraordinary reliability of individual sub-cell materials has made them more advantageous. Additionally, it's crucial to examine the strength of the subcell interface layers, which varies depending on the terminal arrangement as depicted in Fig. 1. NREL, for instance, has employed accelerated testing, such as heat cycling, to investigate the prolonged proficiency of the TCA that may be further employed to electrically pair up 2T and 3T tandems as it becomes the novel part of the production of PV cells. However, research on module-level degradation should mainly be used in conjunction with analysis on cell-level degradation. This demonstrates an important limitation of 3T and 4T designs, indicating the necessity for a more complex cell interconnection mechanism than the commonly used series-interconnection method for SJ and 2T cells [15].

Currently, the 2T series connection method is employed in all commercial-level solar cell designs depicted in Fig. 2(a).

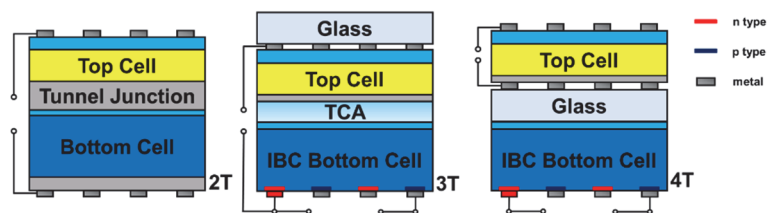


Fig. 1. Terminal arrangements of III-V based Si tandem solar cell adapted from [14] with the permission from publisher.

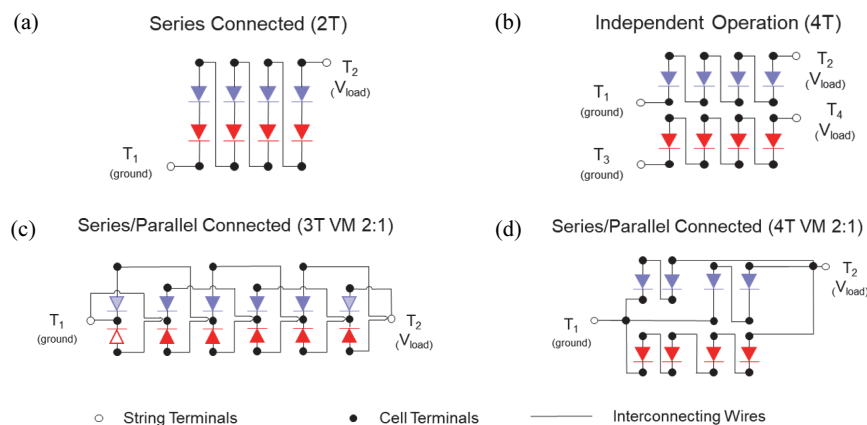


Fig. 2. Cell interconnection scheme [14] published with the permission from Publisher, where (a) indicates the series connection of 2T, (b) independent operation of 4T, (c) series/parallel connection of 3T with 2:1 voltage matching as well, and (d) series/parallel connected of 4T with 2:1 voltage matching respectively (It is also feasible to use different ratios of voltage matching (VM). It should be noted that in the 3T case, end losses, which run at lower power in the open or partly colored cells are evident).

While connecting multiple 2T SCs further needs a connection in series, there are different ways to link 4T and 3T cells. The 4T tandem cells can be powered by two separate series-connected strings as shown in Fig. 2(b), each of which needs intricate module and system integration, and outstanding dielectric isolation exhibits between the sub-cells to retain electrical independence. With a series/parallel methodology, the terminals of two module-level are used to link 3T cells, as shown in Fig. 2(c), however, each sort of 3T cell may need a different string layout. Alternately, 4T cells can be linked together in strings utilizing parallel and series circuits that give two terminals of module-level T1 and T2 as shown in Fig. 2(d), enabling the integration of system-level correspondingly to that of 2T modules joined in series [16].

Furthermore, the string circuitry may be modified to operate at subcell voltages in both series and parallel circuits. Figures 2(c) and (d) show the interconnection configurations with a 2:1 voltage matching (VM) ratio, where the top cell voltage is twice of bottom cell (however, there might be a lot of other ratios). Every time a 3T string connects to a single load, current collection end losses will occur as well. Since not all the electricity from these subcells is being gathered, Fig. 2(c) shows the open or partly colored diodes at the string end. However, the power loss for a string of 60 cells might be as much as one tandem cell, or 1.6%, depending on how the cells

are manufactured. Several III-V/Si tandem device connectivity designs have undergone performance simulations (supposing real materials, without any connection losses, and unlimited strings). Furthermore, 3T parallel/series-interconnected arrangement for a 1.81 eV GaInP/Si with a 2:1 voltage matching ratio, the 3T string was just as efficient as the 4T in almost all cases. The estimated energy yield for the 2T design was 33% (considering AM 1.5G), while the expected energy generation was recorded above 36% for the 3T and 4T designs and therefore showed small sensitivity to spectral deviations. The simulations demonstrate the ideal connectivity technique for tandem cells, which may vary in their application (i.e., terrestrial or space). However, it is important to conduct outdoor tests using small modules made of III-V/Si tandem SCs coupled in 3T and 4T setups to assess this technology's reliability and performance over the long term [15,17].

3. MECHANISM OF GROWTH

Different techniques for combining III-V composites with Si in III-V/Si tandem SCs are studied such as heteroepitaxial growth, wafer bonding, and mechanical stacking [18]. Owing to their lattice and thermal mismatch, the III-V composites' heteroepitaxial development on Si substrate is complicated.

Table 1. Comparison of different configurations of 2T, 3T, and 4T tandem solar cells.

Terminals	Characteristics
2T	<ul style="list-style-type: none"> • Current matching of subcells is necessary. • It reacts to spectral changes. • It is suitable to be utilized as commercial cells. • It is simple to link in parallel and series connections, making module integration easier. • By eliminating the intermediate electrode, it reduces parasitic absorption.
3T	<ul style="list-style-type: none"> • It consists of two interconnected networks. • Current matching is not necessary. • It can withstand spectrum fluctuation. • Intermediate grids are not necessary. • It is inconsistent with direct growth on the bottom subcell.
4T	<ul style="list-style-type: none"> • There are two separate networks. • Current matching is also not essential. • It contains lower spectral sensitivity. • Shading loss from intermediary grids happens. • Each subcell's effectiveness can be increased.

Even so, this could be the most affordable path to integrate tandem III-V/Si SCs [19]. However, the only III-V compounds that are comparable with the Si lattice are GaAs and Ge, respectively. Due to this, it is challenging to manufacture tandem SCs employing III-V compound heteroepitaxial growth on substrates of Si. It is possible to incorporate lattice-matched III-V tandem SCs having better crystal features utilizing the GaAs or Ge as substrates from III-V materials by connecting independently treated Si and III-V materials via direct wafer bonding or mechanical stacking methods, exhibits the perfect solution to the heteroepitaxial problem [20]. With intentions to be more cost-effective, it requires to be paired with a way to reuse the III-V substrates, like epitaxial lift-off or spalling. Mechanical stacking also eliminates the requirement for polished contact surfaces for sub-cell integration. This means that the sub-cell interface may make use of textured Si [21,22]. Furthermore, the three techniques for growing III-V compounds are discussed here.

3.1 III-V compounds on si substrate: direct heteroepitaxial

Because of the mismatch between the lattice and thermal behavior of the two materials, as previously described, III-V on Si based direct heteroepitaxial growth is exceedingly complicated. However, now, this technique is the most economical for incorporating the III-V/Si tandem SCs. Typically two processes are involved in direct heteroepitaxial growth: a low-temperature procedure (400 °C) and a high-temperature process (600–750 °C). In low-temperature process, generally, a thin film of III-V material (often GaAs) of thickness 10–15 nm is formed and used as a nucleation layer [23]. The epitaxial layer uniformity is then further enhanced by a high-temperature process. High defect densities between the III-V compounds and the substrate of Si remain a continual issue even after the two processes mentioned above. Therefore, several strategies, such as thermal cycle annealing (TCA) and strained-layer superlattices (SLS), are advised to further decrease the defect density [24,25].

Figure 3 depicts the GaAs SCs manufactured via metal-organic chemical vapor deposition (MOCVD) method [26] on a Si substrate. Employing MOCVD (having a low environment pressure) facilitates the heteroepitaxial production of III-V material (GaAs) on Si substrates with a 0.5–2° inclination.

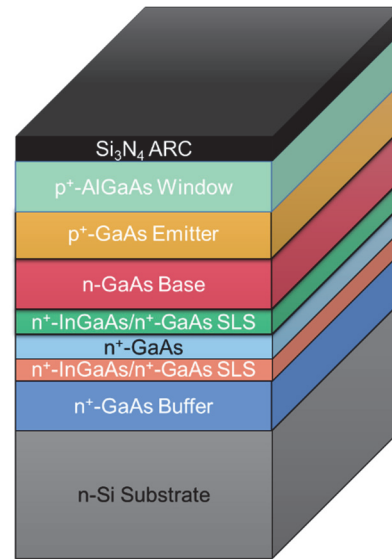


Fig. 3. Schematic depicting the constituents of high-efficiency GaAs/Si tandem solar cell [12] and published with the permission from Publisher.

There are three phases involved in heteroepitaxial growth. Before inserting the Si substrate into the reactor, it must first be etched and degreased. The substrate is therefore preheated with a 1,000 °C hydrogen flow for 10 minutes to eliminate contaminations and oxides from the surface of the Si. Lastly, GaAs layers are deposited on annealed GaAs/Si by employing the TCA and SLS insertion procedures as well as III-V compound direct heteroepitaxy growth on the substrates of Si.

Nowadays, utilizing buffer-graded layers to provide III-V compounds access to Si lattice constants are mainly focused [26]. The lattice constant of III-V materials deposited on Si substrates however is the same since their compounds eventually changed to those needed for III-V compounds (or very close to it). Herein, the $\text{Si}_x\text{Ge}_{1-x}$ and $\text{GaAs}_y\text{P}_{1-y}$, the two significant graded buffer layers, are discussed briefly.

3.1.1 Graded $\text{Si}_x\text{Ge}_{1-x}$ buffer

The step-graded $\text{Si}_x\text{Ge}_{1-x}$ buffers provide a few benefits. The most important benefits of the Ge layer generated on the Si substrate are good features/quality, low threading dislocation density (TDD), as well as relaxation, making it an excellent Ge foundation for the development of III-V combinations (basically GaAs).

SiGe buffers have been effectively employed by organizations and companies all over the world to integrate

III-V compound materials onto Si substrates. Some of the growth processes employed in this methodology are MOCVD, molecular beam epitaxy (MBE), and ultra-high vacuum chemical vapor deposition (UHV-CVD) [27]. To get III-V tandem SCs to operate on the substrates of Si, typically two steps must be taken, however, the SiGe buffer, as well as the development of the GaAs layer, are both established by this. First, using UHC-CVD, a projected 12 μm thick SiGe buffer thin film with a step-graded arrangement is deposited on (100) Si. Then, by cutting the real (110) plane via 60°, this layer was transformed into a 100% undisturbed Ge film (TDD of the Ge layer is $2.1 \times 10^6 \text{ cm}^{-2}$). Therefore, the epitaxial layer of Ge is then deposited via the MBE process, and the second layer of GaAs is subsequently deposited on top of the Ge layer using the same technique [28]. The evolution of a single junction p/n GaAs solar cell having a step-graded $\text{Si}_x\text{Ge}_{1-x}$ buffer layer is shown in Fig. 3. According to [29], the cell proficiency of this solar cell is 18.1% under AM 1.5D conditions and 15.5% under AM 0 conditions. The solar cell with a SiGe substrate as shown also has a high productivity that is almost unaffected by the area of the cell. This makes the issue of the temperature mismatch between the Si substrate and GaAs epitaxial layer easier to solve.

3.1.2 Graded buffer of $\text{GaAs}_y\text{P}_{1-y}$

The lattice parameter of GaP is remarkably like the Si, indicating about GaP that it might be a great option for III-V material direct heteroepitaxy growth on the Si substrates. Additionally, by doping arsenic into GaP and adjusting the arsenic ratio, one can generate a ternary $\text{GaAs}_y\text{P}_{1-y}$ whose lattice characteristics are nearly identical to those of the III-V combination.

Due to the inclusion of a buffer layer in between the material (compound) coated on the top of the Si substrate, certain top material lattice qualities will be required. However, the bandgap needed for tandem SCs top material required be 1.5 eV or 1.7 eV, respectively [27]. Unfortunately, there are not many options for the top layer that can match these standards, hence for 2 J and 3 J tandem SC the GaAsP as well as GaInP/GaAsP is the only option available. Also, it is very hard to grow Si substrates with high-standard GaP despite the lattice parameters of GaP as well as Si being the same. When developing polar GaP on pure nonpolar Si substrates, numerous nucleation-related challenges emerge, including

antiphase domains, stacking layer defects, and dislocations. These problems have been solved in a number of ways, such as by putting the index and substrate in the right places and putting nuclei on the inner surface [30,31].

3.2 Wafer bonding

Wafer bonding is recommended in III-V SC films epitaxially grown on the substrate of Si to prevent the cell from fracturing or bending owing to diverse heat coefficients, high dislocation densities, and lattice mismatch. By employing the hydrogen-induced layer transfer approach, Ge wafers are first injected with H^+ ions, and therefore connected to the Si substrate using oxide SiO_2 (i.e., bonding layer). Before beginning epitaxial growth, it is significant to remember that the wafer bonding must be finished. Subsequently, the bonding unit must next be annealed at $250\text{--}350^\circ\text{C}$ and around 10 atmospheres to attain hydrogen-induced layer splitting. However, microcracks in a Ge wafer spread more rapidly when this procedure is applied [32-34].

Furthermore, to create bonded patterns, wafer bonding, and ion implantation-induced layer approach are being used, hence the 2 J GaInP/GaAs tandem SCs on Ge/Si models can perform more effectively as compared to tandem solar cells on epi-ready Ge substrates. However, the consequent post-bonding epitaxial growth and the thermal imbalance between the substrate layer, compound layer, and bonding layer could cause the thin solar cell coating to be susceptible to fracturing. Additionally, GaAs and Si substrates' various thermal expansion coefficients which produce the thermal strain are prevented by this technique, which is a considerable advantage [35]. Additionally, this method has three rather major downsides: the produced film's significant root-mean-square roughness (about 25 nm on average), substantial surface harm that penetrates the interior of the cell (approximately 200 nm), and the solar cell's nominal polar construction (occurred due to the strong polarity and the concentration of doping and the demand for the material interfacial layer). Usually, to fix these flaws, semiconductor wafer bonding techniques are frequently used [36].

3.3 Mechanical stacking

The combination of III-V on Si based mechanical stacking

is depicted in Fig. 4, however, one of the main manufacturing steps by step processes for combining solar cells employing mechanical stacking is hereby shown in Fig. 5. This procedure requires a layer transference technique for the III-V materials layer. The new method is totally wed, allowing this technique to be utilized in high-volume manufacturing conditions [36].

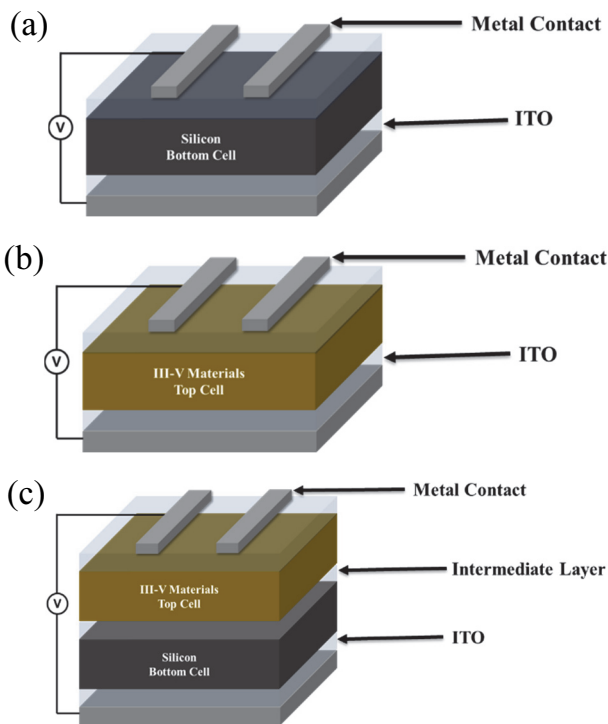


Fig. 4. Combination of (a) Si-bottom cell, (b) III-V as (c) III-V on Si Tandem SCs.

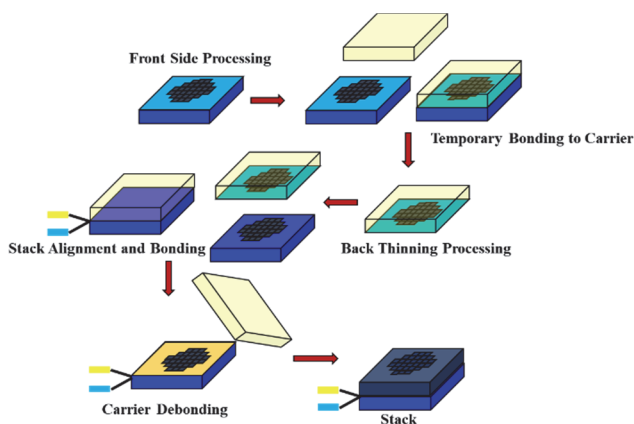


Fig. 5. Indicating the technology of stacking and published with the permission from publisher [12].

Furthermore, as this technology is like the ICs 3D stacking, this technique could benefit tremendously from the promptly growing domain of 3D integration as well. Hence, a III-V-on-Si tandem SC is integrated by combining III-V materials with Si substrate via mechanical stacking, which entails adhering of the III-V materials and Si substrate together. This method results in the formation of chemical bonds between the III-V compound and the Si substrate because the bonding materials are effectively prevented from having lattice dislocation flaws [37]. Considering that most Si sub-cells and III-V compounds both require terminals, the actual bonding materials employed are insulating, or non-conductive, which may impose further expenditures.

4. COMMERCIALIZATION STRATEGIES FOR III-V/Si TANDEM

The highest PCE acquired via reproducible test circumstances is a critical requirement for developing tandem technologies. For an III-V/Si tandem SC to be economically feasible, its efficiencies must exceed 30% (AM 1.5G) to absolve the higher price and intricacy. The concentration should move from lab-certified performance to energy yield if an III-V/Si cell structure can attain a PCE of 30% [13]. Energy yield gives attention to the real-world factors which can affect the effectiveness, like solar irradiance, sample alignment, temperature, etc. Data acquired from a cell's outdoor proficiency is necessary for the very accurate estimation of energy yield [37]. Researchers will need to recognize the cell structures able to consistently achieve high PCE and then examine the continuing outdoor behavior of these cells to transform lab-scale prototypes to useful tandem cells for commercialization [38].

Depending on the targeted market, cell designs may have to be adjusted for particular purposes. Solar cells in space may serve as an early market for III-V/Si tandem SCs by boosting the working of III-V PV technology for satellite uses [39,40]. Significant interest is presently focused on low-Earth-orbit satellites because they have the potential to offer lower response time and a stronger signal (for broadband uses) than geostationary satellites. High power (i.e., watts produced per solar array mass or W/kg) could be delivered by III-V/Si SCs, as they indicated excellent PCEs. However, the most

important factor will be evaluating the working of a prototype cell under continued exposure to the harsh circumstances of the space atmosphere. NASA acquired a 4T GaInP/Si tandem solar cell from NREL and the Institute for Solar Energy Research in Hamelin for study as part of the Materials International Space Station Experiment. After extensive exposure to the sun on the exterior of the International Space Station (ISS), this cell including eight other different models from NASA and US-based scientific organizations will be returned to Earth. These types of investigations can discover substantial degradation patterns in space, which can be used to improve cell designs for space power applications [13,40].

In addition to studying degradation in space, it is therefore very important to examine the III-V-on-Si tandem SCs degradation in diverse weather conditions to determine whether design adjustment is required for terrestrial significance. However, early global market targets for III-V/Si tandem SCs may contain building-incorporated PV, and vehicle-incorporated PV, including different further power production uses, whereas the area limitations are therefore the main problem (Fig. 6). The premium for module efficiency is expected to rise as future PV markets become even more space-constrained than current ones.

To contend with Si PV (the market-leading), this technique must significantly decrease the expense of III-V/Si tandem to achieve the ideal combination of maximum efficiency and low cost. The usage of the inexpensive substrate and III-V deposition method cost reduction are therefore the two primary research extents that influence the cost. Recent research compared the performance of two 4T GaAs/Si tandem

SCs having identical top cell arrangement: One of the top cells is made of GaAs using organometallic vapor phase epitaxy (OMVPE), while another top cell is formed through hydride vapor phase epitaxy (HVPE). Within the limitations of measurement uncertainty ($\pm 3\%$ absolute), according to NREL the declared PCE of the HVPE-grown and OMVPE-grown GaAs top cells had efficiencies of 23.4% and 23.7% (1-sun, AM 1.5G) which are regarded equivalent respectively. This report demonstrates that III-V materials generated by inexpensive deposition processes could offer feasible options to OMVPE for the creation of III-V-on-Si tandem solar cells with high efficiency. Substrate re-use procedures (with little refining) provide an additional major area of cost-reduction research. To significantly lower prices, new inexpensive substrate techniques (i.e., those having a cost equivalent to Si) must become accessible. This might be accomplished by drastically reducing the cost of the GaAs substrate developing a novel substrate material, or III-V cell on Si direct growth hence removing the requirement for an III-V substrate. However, direct growth on Si is possible for 2T and 3T cells, but unsuitable for 4T devices. All of these are possible ways to reduce substrate costs, though, need more research and development [16,17].

Research emphasizing the generation of energy must employ inexpensive fabrication methods for top cells of tandem solar cells and therefore small modules must be built for continuing on-sun investigation to verify that the decline of cost can be turned into energy output. The next stage for 4T designs will be to research the most efficient way to connect tandem solar cells into a small module with minimum complication and failure. To create a prototype proof-of-concept for 3T cells that can experimentally verify predicted simulated efficiencies, the 3T cells should keep focusing on achieving efficiencies of more than 30% having III-V as top cells. Research should concentrate on the continuing energy production of small modules made from 3T III-V/Si tandem SCs having the upper cells produced by inexpensive deposition once efficiencies of more than 30% can be proven with 3T cells [17,41].

III-V/Si tandem SCs have shown the efficiency parallel to those of all-III-V tandem cells. Hence, the attention and further advances of this technique is therefore required to change from high PCE under STC to enhancing energy generation, lowering costs, and displaying novel device

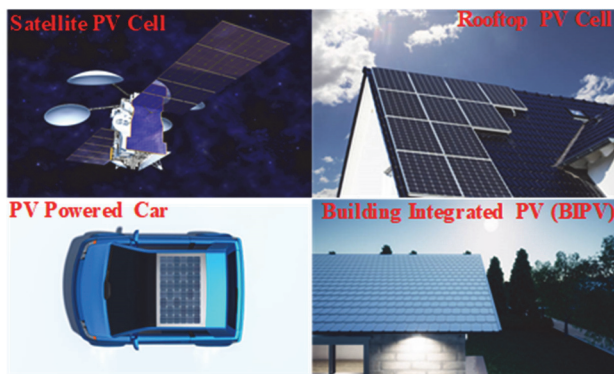


Fig. 6. Potential market target of III-V on Si tandem solar cells, achievable via 2T, 3T, and 4T cells.

Table 2. Represents the performance of different III-V materials employed as an active layer in tandem solar cells.

Year	Cell structure/material	Tandem cell efficiency η (%)	References
2010	GaInP/GaInAs/Ge & GaInP/GaAs/Ge	27.0 & 29.2	[42,43]
2012	GaInP/SiGe lattice-matched tandem: 2-T, S-T	29.1 & 37.9	[44]
2014	Thin-film, flexible, InGaP-GaAs tandem solar Cell	30.8	[21]
2015	III-V//Si tandem solar cells: 2 J, 3 J	38, 43	[45]
2016	GaInP/GaAs//Si triple-junction cell	30.2	[46]
2017	InGaP/GaAs//Si cells	24.5	[47]
2019	GaInP/Si tandem cell: 2T, 3T	26.4, 27.3	[48]
2020	GaAsP/Si tandem cell HT-AlGaAsP BSF/HT-GaAsP	25	[49]
2021	AlGaAs & GaInAsP	17.9 & 20.5	[50]
2022	InGaP/GaAs//ClGSe three-junction solar cell	29.3	[51]
2023	Lead-free MASnI ₂ B _{r1} -Si-based tandem solar cell	30.7	[52]

configurations. The main benefits of III-V-on-Si technology are the long-run stability of the materials as well as the possible decrease in overall cost relative to other-III-V devices, however, the capability to incorporate a low bandgap subcell lacking a metamorphic grade, as well as the capability to add IBC contacts for 3T and 4T designs. To find the ideal cell and interconnection strategies for market targets, research must recognize the elements that affect hybrid tandem performance in the field or in space at both the cell and module levels. The commercial feasibility of this technology depends on obtaining an excellent energy yield at the module level, with reliability like its constituent subcells, while achieving significant cost reductions [53].

Finally, Table 2 shows the previously reported efficiencies based on different III-V materials/structures for effective tandem SCs.

5. CONCLUSION

Herein, we report the growth development of III-V materials based on the substrates of Si and their features as tandem solar cells. Therefore, a detailed analysis of terminal configuration i.e. 2T, 3T, and 4T have been presented briefly by analyzing their different operation methods in series and parallel with different voltage/current matching techniques indicating the difference terminal configuration suitable for III-V/Si tandem SCs. Three main growth methods are discussed in the growth mechanism such as heteroepitaxy,

wafer bonding, and mechanical stacking, and unveil their benefits as well as drawbacks of the techniques. However, the growth of the heteroepitaxial layer based on Si substrates the cost-effective procedure for the incorporation of III-V/Si tandem SCs undergoes through a lattice and thermal mismatch between the III-V compound as well as the substrate of Si. Whereas wafer bonding and mechanical stacking are the other two growth techniques discussed in detail, which can resolve lattice mismatch and dislocation issues. Although these techniques also cause further losses which reduces the cell efficiency hereby raises the cost of fabrication. Additionally, the mechanical stacking method can provide distinct benefits due to subcell integration which is not necessary for interface surface burnishing and permits the utilization of textured Si on the subcell interface. However, it is also promising to employ the textured style Si on the interface of subcell because, unlike heteroepitaxy growth and wafer bonding procedures, mechanical stack integration of solar cells does not need the contact surface to be polished for subcell combination. The methods that might be employed to increase the effectiveness of III-V/Si tandem SCs and their gains in everyday uses are thoroughly covered in the commercialization strategies for III-V/Si tandem SCs.

Moreover, there are still huge obstacles with the solar cell architecture and performance factors. Fortunately, this enables different opportunities for the prospective manufacturing of extremely proficient as well as inexpensive III-V/Si tandem SCs. However, more investigation on various growth mechanisms indicates that under concentrated sunlight III-

V/Si tandem SCs boost the PCE to exceed 40%, displaying a bright future for III-V/Si solar cell technology.

ORCID

Junsin Yi

<https://orcid.org/0000-0002-6196-0035>

Suresh Kumar Dhungel

<https://orcid.org/0000-0001-8255-9913>

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