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# Improvement of Storage Performance by $HfO_2/Al_2O_3$ Stacks as Charge Trapping Layer for Flash Memory– A Brief Review

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**Abstract:** As a potential alternative to flash memory, $HfO_2/Al_2O_3$ stacks appear to be a viable option as charge capture layers in charge trapping memories. The paper undertakes a review of $HfO_2/Al_2O_3$ stacks as charge trapping layers, with a focus on comparing the number, thickness, and post-deposition heat treatment and γ-ray and white x-ray treatment of such stacks. Compared to a single $HfO_2$ layer, the memory window of the 5-layered stack increased by 152.4% after $O_2$ annealing at ±12 V. The memory window enlarged with the increase in number of layers in the stack and the increase in the Al/Hf content in the stack. Furthermore, our comparison of the treatment of $HfO_2/Al_2O_3$ stacks with varying annealing temperatures revealed that an increased annealing temperature resulted in a wider storage window. The samples treated with $O_2$ and subjected to various γ radiation intensities displayed superior resistance. and the memory window increased to 12.6 V at ±16 V for 100 kGy radiation intensity compared to the untreated samples. It has also been established that increasing doses of white x-rays induced a greater number of deep defects. The optimization of stacking layers along with post-deposition treatment condition can play significant role in extending the memory window.

**Keywords:** Charge trapping layer, Stacks, High-k material, Non-volatile memory, Memory window

## 1. INTRODUCTION

Non-volatile memory is an integral part of advanced digital portable device in which flash memory based on floating-gate technology dominates the market due to high data transfer efficiency, small size, light weight, strong mechanical stress resistance, and low power consumption [1]. However, the need to keep reducing the storage cell size due to the massive growth in size of stored data has caused the floating gate technology to approach its physical limits [2].

Charge trapping memory (CTM) has received a lot of attention as a viable candidate to replace the conventional floating-gate flash memory because both CTM memory cells and floating-gate cells work on the principle that charge enters or leaves the gate dielectric stack from the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) channel, which is very favorable for CTM [3]. The main difference between CTM and floating-gate is that floating-gate stores electrons in a polysilicon layer (floating gate) between two dielectric layers. While CTM can store electrons directly in discrete charge traps in the dielectric layer [4]. Initially $Si_3N_4$

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layer was used as a charge trapping layer in Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) devices, but the small dielectric constant of $Si_3N_4$ makes the charge trapping less efficient and retention performance of $Si_3N_4$ layer deteriorates as its thickness decreases [5].

In the last two decades, high-k materials with high trap densities have attracted great attention and there have been many studies to confirm their potential as charge trapping layers, such as $HfO_2$, $ZrO_2$, $Al_2O_3$, $Ta_2O_5$, $Y_2O_3$, etc [6-11].Their dielectric constants and bandgaps are shown in Table 1. According to the gate capacitance formula, the value of C can be determined by:

$$C = \frac{(\kappa \times \varepsilon \times A)}{t_{ox}} \quad (1)$$

where κ is the relative dielectric constant, $\varepsilon$ is the dielectric constant, $A$ is the area between the capacitive pole plates, and $t_{ox}$ is the thickness of the oxide layer. After the introduction of high-K dielectric material, the capacitance increases significantly without changing the oxide thickness and other conditions. This demonstrates that the use of high-k materials as charge trapping layers results in higher trap densities and improved storage capabilities for electronic devices. On the other hand, when higher bandgap materials are used without increasing the device thickness, the retention time of large storage windows is extended, which helps to improve the storage performance of the device. Figure 1 shows that applying a positive voltage to the top electrode, electrons enter the charge trapping layer from the tunneling layer due to the tunneling effect. High-k materials such as $HfO_2$ or $Al_2O_3$ captures a large number of electrons, and at the same time, due to the larger bandgap of $Al_2O_3$, it is difficult for the captured electrons to escape, thus achieving a good charge storage effect, in which electrons penetrate the larger thickness of the $Al_2O_3$ blocking layer, with only a small number of electrons able to reach the Al gate through the blocking layer.

One of these materials, $HfO_2$ has received the greatest attention since it can store charges more efficiently than $Si_3N_4$ and can be improved by nano-laminated $HfO_2$ and $Al_2O_3$ charge trapping stacks [12,13]. In this study, the development of $HfO_2/Al_2O_3$ as a charge trapping layer was summarized by studying its structural improvement and post-deposition treatment.

**Table 1.** Comparison of dielectric constants and bandgaps of $Si_3N_4$ and various high-k materials.

| Material | Dielectric constant | Bandgap (eV) |
|---|---|---|
| $Si_3N_4$ | 7 | 5.1 |
| $HfO_2$ | 25 | 5.9 |
| $Al_2O_3$ | 9 | 8.7 |
| $ZrO_2$ | 25 | 5.0 |
| $Ta_2O_5$ | 26 | 4.6 |
| $Y_2O_3$ | 11 | 5.6 |

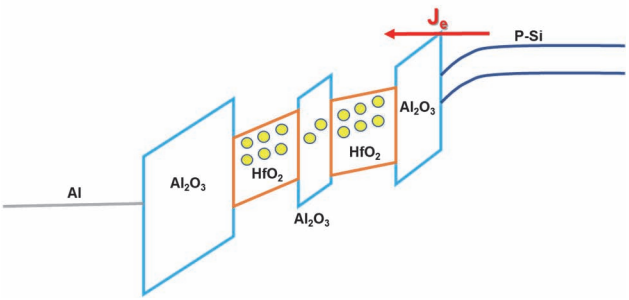



**Fig. 1.** Energy band diagrams of $Al/Al_2O_3/HfO_2/Al_2O_3/HfO_2/Al_2O_3/p$-Si memory structure under program process.

## 2. STRUCTURE AND PRINCIPLE

The fabrication process flow for the $Al/Al_2O_3/[Al_2O_3/HfO_2$ stacks$]/Al_2O_3/Si$ memory devices is shown in Fig. 2(a) and the device structure schematic of $HfO_2/Al_2O_3$ stacks as the charge trapping layer is shown in Fig. 2(b).

As a subset of chemical vapor deposition, atomic layer deposition (ALD) is a thin film deposition technology based on the continuous application of a vapor-phase chemical process. Most ALD reactions utilize two substances known as precursors (also called 'reactants'). These precursors undergo successive, self-limiting reactions with the material's surface one at a time. ALD is a crucial procedure for creating semiconductor devices and is a component of the arsenal used to create nanomaterials. To bring the internal organization of the metal close to equilibrium and obtain good process and serviceable properties, rapid thermal annealing (RTA) is involved for heating the device to a higher temperature, holding it there for various lengths of time depending on the material and size of the device, and then rapidly cooling it. In this paper, the treatment of post-deposition annealing (PDA) in different ambient conditions and temperatures are reviewed.

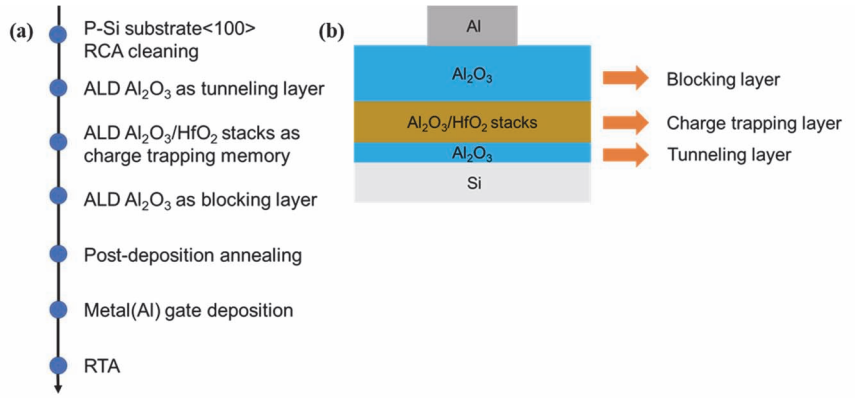



**Fig. 2.** (a) Memory device process flow with $Al_2O_3/HfO_2$ stack as the charge trapping layer and (b) memory device cross-sectional construction diagram.

## 3. RESULTS AND DISCUSSION

### 3.1 Replacement of $HfO_2$ with $Al_2O_3/HfO_2$ stacks

Many studies dedicated to $Al_2O_3/HfO_2$ stacks instead of $HfO_2$ as a charge trapping layer have been explored [14-17]. The X. Xue et al. [18] experimented with a new comparative test to try to add $Al_2O_3$ to the $HfO_2$ charge trapping layer to form a stacked layer. Figure 3(a) showed the variation of the memory window of the unprocessed device at various sweep voltages. The memory window was defined as the difference in flat band voltage ($V_{fb}$) between the programmed and erased states [19]. It could be seen that the memory window of the single layered sample was 1.62 V, which was larger than the 1.48 V for 3 layers and 5 layers. Among the as-grown samples there was higher $HfO_2$ content in the single layered sample than in the samples with 3 layers and 5 layers, where the dielectric constant of $HfO_2$ was larger than that of $Al_2O_3$ [20]. However, it seemed that the situation was reversed after the $O_2$ annealing treatment. Figure 3(b) showed the memory windows of the samples annealed by $O_2$ at 800°C at various sweep voltages, and when the sweep voltage reached ±12 V, the memory window of the 5 layers sample reached 2.55 V, which represented a 152.4% improvement compared to the single layered sample and a 30.8% improvement compared to the three layered sample, indicating that the number of stacked layers in the charge trapping layer had a positive effect on charge storage capacity, It simply means that more the number of layers that are stacked, better becomes the charge storage capacity [21].

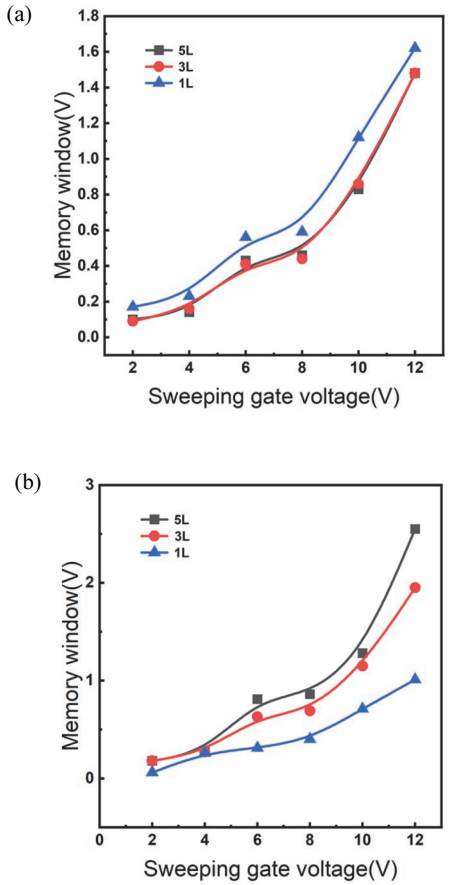



**Fig. 3.** (a) Variation in the memory windows of the as-grown samples with different sweeping gate voltage and (b) variation in the memory window with sweeping gate voltage at 800°C [18].

### 3.2 Change in the Al/Hf ratio in the $HfO_2$/$Al_2O_3$ charge trapping layer

According to Albena Paskaleva et al. [22] merely a little amount of Al doping reduced the traps connected to $HfO_2$'s reduced oxygen vacancy traps. On the contrary, the introduction of a larger amount of Al in the $HfO_2$ membrane increased the trapping capacity of the stack due to the introduction of deeper $Al_2O_3$ related traps. The findings suggested that by adding the appropriate amount of Al to $HfO_2$, the high-k layer's electrical and dielectric properties could be adjusted to satisfy application-specific requirements.

D. Spassov et al. [23] explored the effect of different $HfO_2$ thickness and the different $Al_2O_3$ contented on the trapping ability of devices, and thicker $HfO_2$ exhibited stronger hole trapping, which was shown in Fig. 4(a) as a larger memory window. This implied that defects in amorphous $HfO_2$ were more favorable for hole trapping, a finding that had been confirmed elsewhere [24]. Figure 4(b) showed that electron trapping was stronger in $Al_2O_3$, with a 71% improvement in the memory window for a 5 × (20: 10) sample compared to 5 × (20: 2) at ±15 V.

### 3.3 Post-deposition treatment for enhancement of $HfO_2$/$Al_2O_3$ charge trapping layer

The post-deposition processing (RTA or radiation) seemed to be a huge storage capacity boost for the memory. Since S. Maikap et al. [25] had already obtained the HfAlO nanocrystals by PDA in $N_2$ at 900℃ for 60s. Hou et al. [26] investigated the change of memory window by varying the thermal annealing temperature in $N_2$, annealing at 1,000℃ and 450℃, respectively. Figure 5 showed that the memory window of the sample PDA at 1,000℃ was enhanced by 20.2% compared to the sample PDA at 450℃ with a sweep voltage of ±8 V, and this value was 5.5% at a sweep voltage of ±12 V. The enhanced charge trapping ability of the sample at 1,000℃ should be attributed to the formation of HfAlO nanocrystals, where $HfO_2$ and $Al_2O_3$ were highly mixed.

Dencho Spassov et al. [27] explored the effect of γ-radiation on $Al_2O_3$/$HfO_2$ stacks and its memory window through the most common source of the γ-radiation, cobalt-60 ($^{60}Co$). Figure 6(a) and (b) showed that PDA in $O_2$ was favorable for the memory window of the $Al_2O_3$/$HfO_2$ stacks, and this

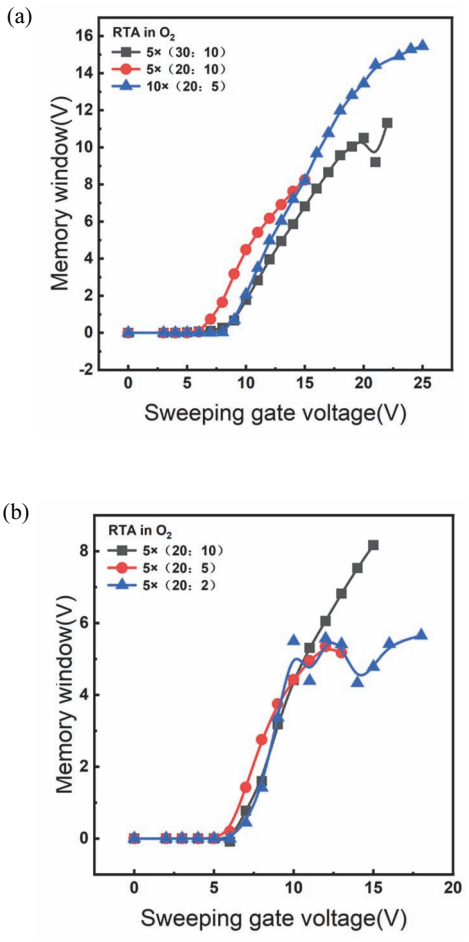



**Fig. 4.** Variation of device memory window: (a) different $HfO_2$ sublayers thickness and (b) different $Al_2O_3$ content [23].

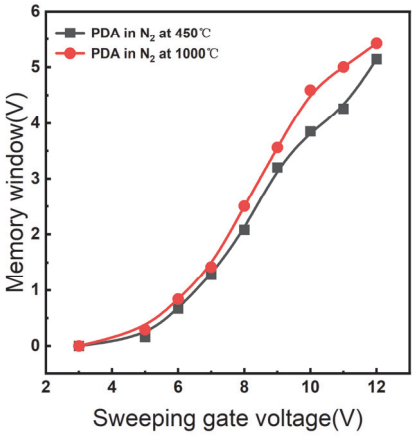
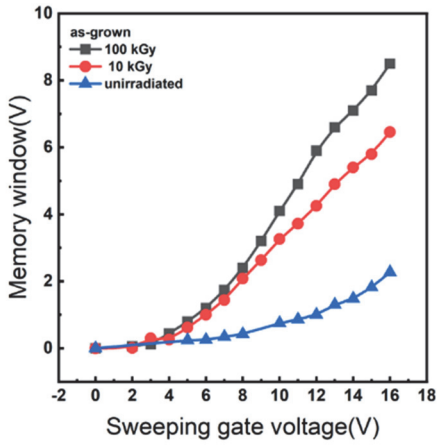
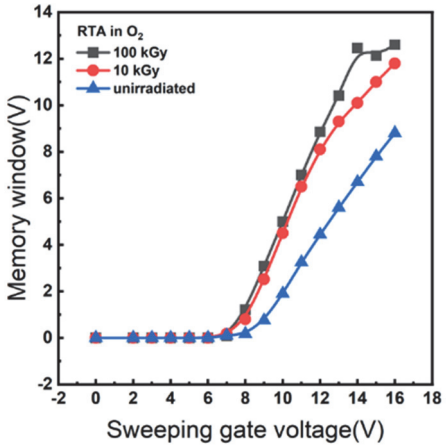



**Fig. 5.** Memory window of the device in different temperatures of the $N_2$ PDA [26].

(a)




(b)




(c)

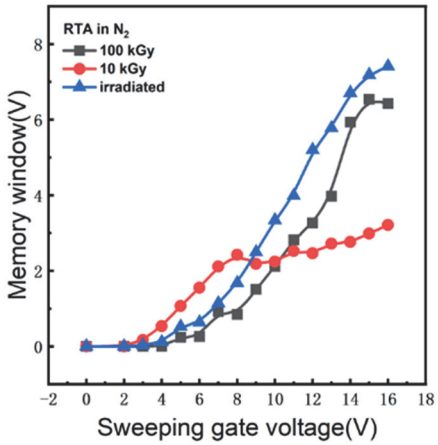



**Fig. 6.** The evolution of the memory window when voltage pulses of different $V_p$ were applied before and after radiation: (a) as grown, (b) PDA in $O_2$, and (c) PDA in $N_2$, respectively [27].

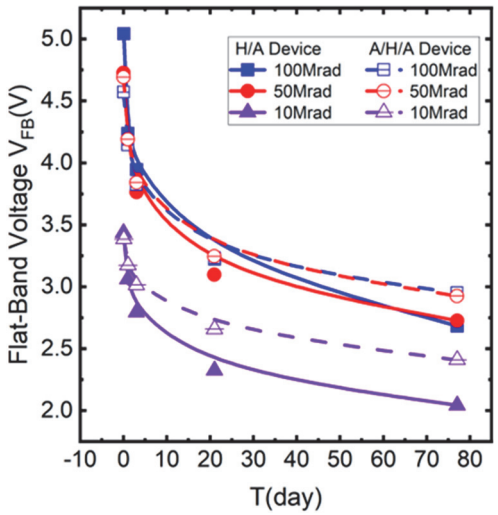



**Fig. 7.** Variation of flat-band voltage with room temperature annealing time for $HfO_2/Al_2O_3$(H/A) devices and $Al_2O_3/HfO_2/Al_2O_3$ (A/H/A) devices at different radiation intensities [29].

conclusion was confirmed by Jinhyuk Yoo et al. [28]. As for the effect of γ radiation, the samples as-grown and PDA in $O_2$ seemed to show good radiation tolerance. Even the memory window increased significantly due to the generation of new electron traps, with 274.4% increase in the memory window of the as-grown sample at a high radiation intensity of 100 kGy with a sweep voltage of ±16 V compared to 43.2% for the sample PDA in $O_2$. It was noteworthy that the memory window of the traps due to PDA in $O_2$ and radiation-induced traps may have the same origin with a memory window of 12.6 V. In contrast, for PDA in $N_2$, Fig. 6(c) showed that the reaction of the stacks under radiation was more complex. After exposure in γ- radiation, the formation of HfON suppressed the radiation-induced charge vacancies, electron capture capability was compromised, and the memory window was reduced.

Hongda Zhao et al. [29] investigated the flat-band voltage of two types of stack devices, $HfO_2/Al_2O_3$ (H/A) and $Al_2O_3/HfO_2/Al_2O_3$ (A/H/A), following exposure to white x-ray radiation. They evaluated the capacitance-voltage (C-V) characteristics of the devices and found that the memory window (flat-band voltage) remained nearly the same for both devices under x-ray radiation less than 50 Mrad. However, for x-ray radiation of 100 Mrad, the H/A device exhibited a maximum flat-band voltage of 5.04 V, which suggests that a high dose of x-ray radiation can induce a higher number of

defects. Additionally, the A/H/A device demonstrated a slower decay of voltage storage after a prolonged period of room temperature annealing. This result indicated that the presence of additional $Al_2O_3$ layers in the A/H/A device can help protect the memory window, which could also be due to the formation of deeper defects in the device.

## 4. CONCLUSION

This review paper briefly focuses on the effect of the ratio of $HfO_2/Al_2O_3$ stacks that make up the charge trapping layer and the post-deposition treatment process on the device capture capability. It can be concluded that increasing the content of either $Al_2O_3$ or $HfO_2$ in the stack is beneficial for increasing the memory window. In addition, the enhancement of the post-deposition annealing on the capture capability of the stack is significant, but γ-rays significantly reduce the memory window of the samples annealed in $N_2$, while the memory window becomes larger for both as-grown and $O_2$ annealed samples. The exposure to white x-rays can lead to the formation of deep defects in the $HfO_2/Al_2O_3$ stacked device, thereby enhancing the memory window. The electrons that are trapped in these deep defects remain stable and do not leak during a prolonged period of room temperature annealing, which provides theoretical support for the operation of the devices in some specific environments. As there seems to be not much work reported on treatment of post-deposition stacks with ultraviolet (UV)-radiation, it may be a future direction for research.

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